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M9 features 64 MBytes of 128-bit wide DDR video memory running at 200 MHz. Combined, this provides graphics power approaching that of a high-end desktop workstation, all on a PMC module. SBS routes the video capture streams through a configurable FPGA to provide the design flexibility designers need for today's systems.

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COTS (kots), n. 1. Commercial off-the-shelf. Terminology popularized in 1994 within U.S. DoD by SECDEF Wm. Perry's "Perry Memo" that changed military industry purchasing and design guidelines, making Mil-Specs acceptable only by waiver. COTS is generally defined for technology, goods and services as: a) using commercial business practices and specifications, b) not developed under government funding, c) offered for sale to the general market, d) still must meet the program ORD. 2. Commercial business practices include the accepted practice of customer-paid minor modification to standard COTS products to meet the customer's unique requirements.

—Ant. When applied to the procurement of electronics for the U.S. Military, COTS is a procurement philosophy and does not imply commercial, office environment or any other durability grade. E.g., *rad-hard components designed and offered for sale to the general market are COTS if they were developed by the company and not under government funding.*

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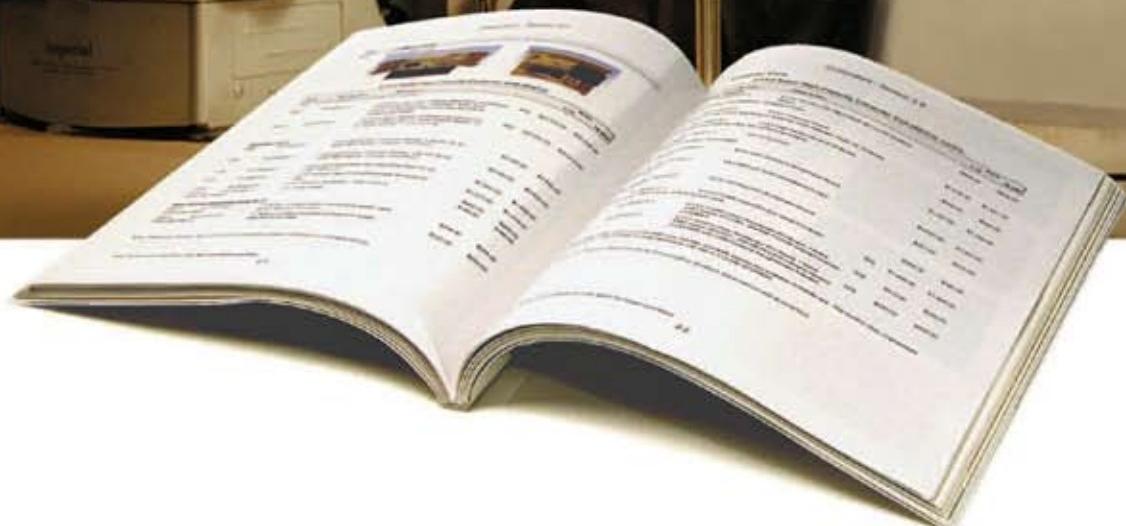
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The amphibious assault ship USS Bataan (LHD5) shown underway with all eight MV-22 Osprey assigned to Marine Tiltrotor Operational Test and Evaluation Squadron 22 (VMX-22), "turning" and ready for takeoff. VMX-22 is conducting the final operational test phase of the tiltrotor aircraft. The MV-22 is an advanced technology, vertical/short takeoff and landing (VSTOL) multipurpose tactical aircraft, and is scheduled to replace aging CH-46E Sea Knight and CH-53D Sea Stallion helicopters currently in service.



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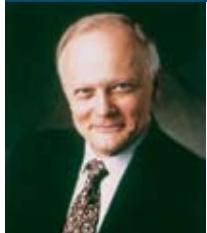
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Publisher's Notebook



Have you ever had a month where dozens of relatively "small" events kept you from achieving most of what you had planned? That's been my last month. So rather than preaching about one subject this month, I'll hit several "small" topics that need some airing.

Let's start with RoHS (Reduction of Hazardous Substances): a noble concept with the health of humanity as its goal. Europe has grabbed the bull by the horns and forced the issue with a July 2006 deadline. But there's one major problem: all the technical problems, such as tin whiskering, haven't been resolved and won't be by the deadline. I was at a conference last May where the Defense Microelectronics Activity (DMEA) provided a series of presentations covering the problems facing the military and space hardware designers if they use RoHS components and systems. I'm sure that there are readers that will disagree and say these potential problems are over exaggerated and remind me that RoHS has an exemption for the military.

Remember, however, that the military market is minuscule with respect to the overall electronics market. No major manufacturer will run parallel production lines, one for leaded and one for unleaded. If your cell phone dies because of an RoHS problem, you go buy a newer, better model and it's an excuse for the upgrade. If your life support system fails in the hospital or your FLIR (Forward Looking InfraRed) system fails while doing a combat run, it's completely different.

If the U.S. can stand its ground against the rest of the world for things like putting carbon dioxide in the air, why can't Congress just pass a law that says that any product sold in the U.S. that fails because of implementing RoHS, the manufacturer is fully liable for any direct and consequential damages? I bet every manufacturer would put two production lines in place, from Beijing to Paris to New York. There would also be a monumental effort to find a technical solution that would satisfy both Europe and the U.S. as quickly as possible.

Is it just me or are we being inundated by useless information overload? When we have a hurricane we have a couple dozen television/cable channels doing 24/7 coverage from every village within the projected cone of impact. Remember when the cable weather channel just told you what the weather was, not stories about the weather? If there's a Supreme Court nominee the news hounds are interviewing the nominee's third grade teacher and fifth cousins. How about what they do with every new movie? And I use the word movie very loosely—anything that doesn't look like a cobbled-together feature-length TV show is sheer accident. It's not just morning and late night talk shows, it's every

show. You tune one in and every actor for each movie released will do the rounds, giving the sales pitch for their movie. And another thing...can't any of the reporters—again using a word very loosely—ask an intelligent question? What do they expect for an answer when asking the question: "and how did you feel when your child was killed?"

I can assure you that no matter what the subject, that's the type of question they'll ask. I never heard Walter Cronkite ask such a question, but then he never went for the current news hounds "money shot": "let's see if we can get the interviewee to cry."

Moving on to the Internet. I almost miss getting all those daily dozens of emails I used to get about how my body could be enhanced, or how I qualified for re-mortgaging my house. Now I get email letters about every product under the sun. I've gotten so desensitized to these things that I normally don't notice what's on them as I delete them. But yesterday while trying to fix a dial-up problem—yeah, yeah, I'm getting a high-speed connection soon—I noticed that I got three email letters from three different sources promoting the same manufacturer's product. How much of this can people take before it just becomes white noise? This situation can't be unique to just me. I need to stay aware of what is going on in our industry and people developing systems need to do the same. So we can't use a SPAM filter because it would keep us from getting what we need.

OK, I'll stop whining. As we exit 2005 and move on to the next year we have some great news. Last year we increased our print circulation of *COTS Journal* from 20,000 to 30,000. And we will now provide a digital edition—not just online articles—of *COTS Journal* that will be a "complete" downloadable PDF version of each issue. That will enable readers in the most remote areas of our planet to get this magazine and enjoy it just as our print readers do. This is only one of several things we are doing to enhance *COTS Journal*. ■■

Pete Yeatman, Publisher
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COTS Journal

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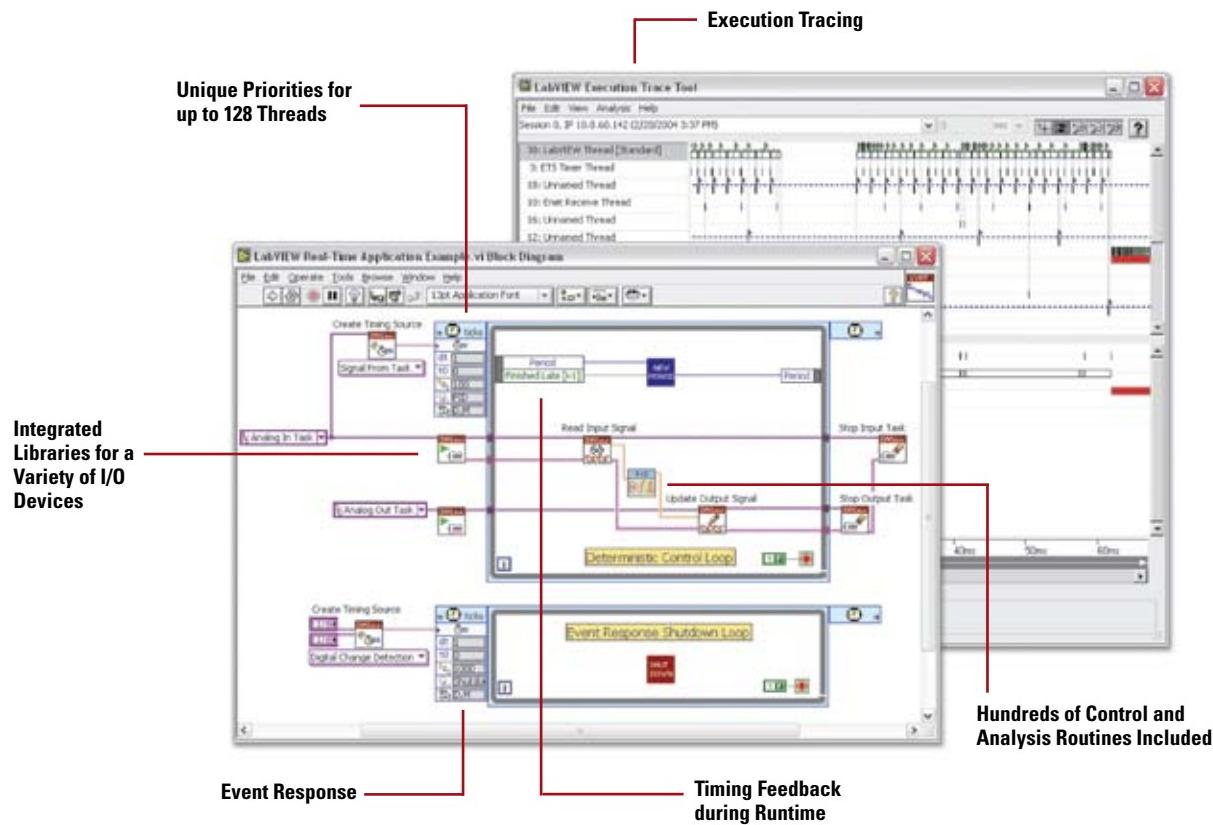
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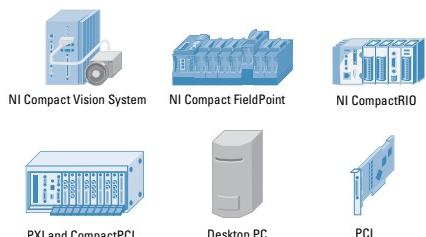
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The Inside Track

TEK Micro Selected to Build Data Acquisition Gear for E-2D Advanced Hawkeye

TEK Microsystems announced that it has received orders totaling \$5 million from Northrop Grumman to produce data recording and playback systems to support the next-generation radar system being developed for the E-2D Advanced Hawkeye. These contracts, the largest award in TEK Microsystems' history, will extend through the first half of 2006. The next-generation E-2D Advanced Hawkeye aircraft will be the U.S. Navy's next-generation airborne early warning and battle management system. The E-2D Advanced Hawkeye will be the latest version of the Hawkeye family of aircraft and will feature a new radar system along with other advanced capabilities. Figure 1 shows the E-2D's predecessor, the Hawkeye E2-C. Currently under development for the Naval Air Systems Command by Northrop Grumman-led Advanced Hawkeye industry team, the E-2D is expected to have Initial Operational Capability in 2011.

Data recording and playback systems for the E-2D will be based on TEK Micro's Jazz-

Store family of data recording solutions. The Jazz Store family of data recording and playback systems includes several capabilities that were critical for the E-2D Advanced Hawkeye application. Among these were an ability to scale up to dozens of modular, heterogeneous input/output channels and FPGA-based

protocol engines to support application-specific processing in real time during record and playback. TEK Microsystems will be delivering a complete systems solution to Northrop Grumman, including deployed flight systems using ruggedized air transport rack (ATR) chassis, laboratory and playback systems, flight test equipment, and ground systems to perform transcription and post-processing of mission data.

TEK Microsystems
Chelmsford, MA.
(978) 244.9200.
www.tekmicro.com.



Figure 1

Designed for missions that rely heavily on radar data recording, the next-generation E-2D Advanced Hawkeye aircraft will be the U.S. Navy's next-generation airborne early warning and battle management system. The E-2D Advanced Hawkeye will be the latest version of the Hawkeye family of aircraft and will feature a new radar system along with other advanced capabilities. Shown here is the E-2D's predecessor, the Hawkeye E2-C. (Photo courtesy Northrop Grumman.)

National Technical Systems Expands Satellite and Launch Vehicle Test Capabilities

National Technical Systems, a provider of quality, conformance and certification testing, quality registration and managed services, has announced an expansion of its specialized tests for satellite and launch vehicle systems and components. The launch simulation tests combine

extremely high-level acoustic noise, vibration and thermal shock to detect failure modes that could impair a launch or result in functional failures in space. The atmospheric tests expose test specimens to gases known to cause long-term degradation of certain materials. The atmospheric tests are combined with thermal shock and solar radiation over long periods to evaluate the survivability of satellite components and systems

designed to operate for many years in space.

Test specimens for the atmospheric survivability tests include components and systems for commercial and military satellites, including solar panels, solar wings, reflectors and pressure storage tanks for fuel cells. Customer requirements for an inert atmosphere required NTS to develop custom ambient-pressure thermal cycling chambers in order to maintain a dry inert

atmosphere while cycling at accelerated rates of up to +/-125°C per minute between +150°C and -180°C. The chambers, which range from 27 cubic feet to 96 cubic feet, replicate space conditions with oxygen levels of less than 50 parts per million while maintaining the dew point below -45°C during the tests. Tests run for months with over 15,000 thermal cycles.

National Technical Systems
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AR Worldwide Modular RF to Supply Booster Amplifiers for Humvees

AR Worldwide Modular RF has announced that it has received an order from Amron International for 71 tactical communications amplifiers. The order, for model KMW1030, a 20W, 512 MHz amplifier, is the latest in a series of orders from Amron, and is unique in that the amplifiers ordered are specifically for use in "Humvee" fighting vehicles rather than as Man-Pack units. The customized units incorporate additional line filtering and spike suppression so that the amplifiers can operate directly off the main vehicle's 24-volt battery system.

Military standards for 24-volt vehicle systems are very demanding, requiring that equipment be capable of working without damage in both under- and over-voltage conditions. The over-voltage conditions are especially demanding since the unit must function with voltage peaks of 100 VDC for up to 100 ms. In order to meet those stringent requirements, AR engineers designed additional circuitry



Figure 2

This amplifier (right) is designed specifically for use in Humvee fighting vehicles rather than as Man-Pack units. Shown here (left) is a Humvee driven in a training exercise by Seabees assigned to the Naval Mobile Construction Battalion Two Three (NMCB-23). (Humvee photo courtesy U.S Navy.)

board layouts in record time and have incorporated them into the KMW1030 for future orders.

AR Worldwide Modular RF
Bothell, WA.
(425) 485-9000.
[\[www.ar-worldwide.com\]](http://www.ar-worldwide.com).

BAE Systems Chooses Quantum3D Visual Computer for Bradley A3 Embedded Training

BAE Systems has selected the Quantum3D Thermite Tactical Visual Computer (TVC) for use in its Bradley A3 Embedded Tactical Training Initiative (BETTI). The BAE Systems embedded trainer is designed to enable every Bradley A3 (Figure 3) to provide a range of mission-critical part-task, unit and collective training activities, including conducting virtual gunnery training in multiple environments. Each training system uses Line Replaceable Units (LRU) that include multiple Thermite TVCs to support driver, gunner and commander displays, as well as Close Combat Tactical Trainer (CCTT) Host and Vehicle Interface, Instructor Operator Station (IOS) and One Semi-Automated-Forces (SAF) Testbed Baseline support.

In addition, the BETTI training solution provides capabilities suitable for future training activities, including embedded Tactical Engagement Simulation Systems (TESS), mission rehearsal, robotic-based sensors and C4ISR applications. Thermite TVC is Quantum3D's small form-factor, real-time visual computer that combines low-power mobile CPU technology, advanced embedded 2D/3D graphics subsystem with video capture capabilities in a ruggedized, sealed alloy enclosure with Mil-Spec connectors.



Figure 3

Designed specifically for the Bradley A3 fighting vehicle (shown here), the BAE Systems embedded trainer is designed to enable every Bradley A3 to provide a range of mission-critical part-task, unit and collective training activities, including conducting virtual gunnery training in multiple environments.

The unit is 100% PC-compatible with support for both Windows and Linux operating systems.

For surveillance and sensor applications, Thermite also includes video-capture and video-out functionality, with support for color space conversion, scaling and overlays for NTSC, PAL, S-Video and RS-170A formats. Thermite TVC is available with both solid-state and shock-resistant rotating disk drives and includes comprehensive PC I/O capabilities as well as Ethernet IEEE 802.3 USB 2.0, IEEE 802.11X, Bluetooth, and a range of factory I/O options including MIL-STD-1553B, Fibre Channel, Tactical/Secure Radios and GPS.

Quantum3D
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[\[www.quantum3d.com\]](http://www.quantum3d.com).

U.S. Army Taps Datapath to Support JNN Initiative

The U.S. Army Communications-Electronics Command in Fort Monmouth, N.J. has awarded Datapath a \$96 million firm-fixed-price sole source contract to deliver a total of 157 trailer-based satellite terminals to support the Army's Joint Network Node (JNN) initiative. In addition, Datapath has provided engineering design and certification services to customize the earth terminals to meet the Army's unique mission requirements. The contract also includes associated technical support, soldier training and spares.

Deployed extensively in Iraq, the JNN initiative is a network-centric communications architecture, which provides reliable and portable

communications to the U.S. Army Third Infantry Division, 101st Airborne Division, Fourth Infantry Division and 10th Mountain Division. This \$96 million award expands the existing JNN implementations with deployments to the First Cavalry Division, the 25th Infantry Division, the 82nd Airborne Division and multiple Army National Guard units.

The Datapath solution is built on two custom versions of its Datapath ET Model 3000 Portable for battlefield communications. It provides a mobile satellite telecommunications platform configurable for operation in Ku band frequency, and for simultaneous Single Channel per Carrier (SCPC) / Time Division Multiple Access (TDMA) carrier transmission. The Datapath 3000 is a compact trailer-based satellite earth terminal that enables secure, robust voice and data communications where no infrastructure exists. It delivers a tactical, rugged communications gateway to battalions for Communications on the Quick Halt (COTQH). A third-generation earth terminal, the Datapath 3000 is specifically designed for sustained and reliable field operation with minimal maintenance by forward-deployed warfighters.

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DTIC Web Site Pulls DoD Technology Info into Focus

The DoD's array of technology-related activities, laboratories and information resources is truly vast. Sorting through all of it and keeping it organized is no easy task. The Defense Technical Information Center (DTIC) was fielded to do exactly that, and its Web site is the centerpiece of that mission. The DTIC provides centralized operation of DoD services for the acquisition, storage, retrieval and dissemination of Scientific and Technical Information (STI) to support DoD research, development, engineering and studies programs.

Among its services is a Scientific and Technical Information Network (STINET) Service available to the general public, free of charge. It provides access to citations of unclassified, unlimited documents that have been entered into DTIC's Technical Reports Collection, as well as the electronic full text of many of these documents. Public STINET also provides access to the Air University Library Index to Military Periodicals, Staff College Automated Military Periodical Index, DoD Index to Specifications and Standards, and Research and Development Descriptive



Summaries. DTIC also makes available sensitive and classified information to eligible users who register on the site.

DTIC also hosts a variety of databases. Its Technical Report Database contains nearly two million reports in print and electronic form, conveying the results of Defense-sponsored research, development, test and evaluation (RDT&E) efforts. DTIC has also acquired Library of Congress Federal Research Division records that cover a variety of foreign and domestic subject areas. A Research Summaries Database contains descriptions of DoD research that provide information on technical content.

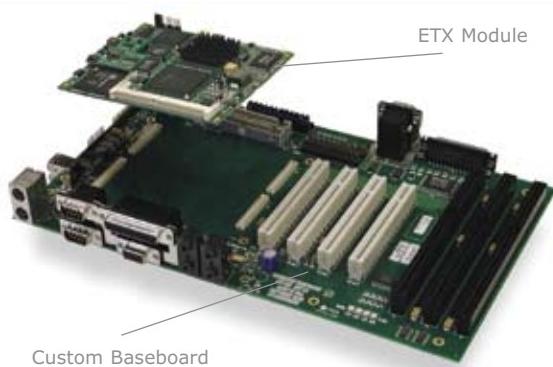
responsible individuals and organizations, principal investigators and funding sources at the work unit level. And finally, DTIC's Independent Research and Development (IR&D) Database has over 165,000 descriptions of R&D projects initiated by DoD contractors but not performed under Federal statute.

Defense Technical Information Center, Fort Belvoir, VA. (800) 225-3842. [www.dtic.mil].

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Hardware Assets

Sensors in the Military

Sensors in the Military: From Battlefield to Barracks

Sensors are being used in growing numbers in a variety of military data acquisition systems. Complex, high-end suites of sensors are being deployed in next-generation components of the Future Combat Systems program, while simpler, low-end devices are found in logistics management and material inventory and control.

Ann R. Thryft
Senior Editor

As the data acquisition needs of today's military expand, sensors are being used in a variety of new and different ways, especially to help improve performance and meet the goals of next-generation electronic combat systems.

In intelligent data acquisition and machine control subsystems, more sophisticated sensors and integrated sensor suites are combining with faster processors and higher-resolution imaging systems to deliver superior capabilities for manned and unmanned applications. The need to process quickly growing amounts of data captured by sensors is pushing hardware limits and affecting the signal processing architectures of data converters.

In the complex environment of the battlefield, multiple potential threats must be accurately and precisely analyzed and assessed using different types of sensors, and then responded to correctly in



Figure 1

Sensors are found in many battlefield applications, including manned and unmanned aerial vehicles (UAVs). This Class I UAV being prepared for takeoff during a Future Combat Systems demonstration is man-portable, and can be fitted with a variety of sensor packages. Photo by Steve Harding, courtesy of U.S. Army.

real time. In the Future Combat Systems (FCS) program, sensors are found in manned and unmanned vehicles, remote operated vehicles, remote and unmanned launch systems and intelligent munitions systems (IMS). The Non-Line-of-Sight Launch System, for example, has self-contained tactical fire control electronics and software for remote and unmanned operations. In a munitions field, the IMS can be armed, turned off to allow friendly forces to pass through, and then rearmed.

Intelligent reconnaissance and surveillance vehicles in the FCS program will feature multiple sensors, including those for infrared, mapping and remote chemical detection. Unattended ground sensors will detect, locate and classify targets, aided by imaging subsystems. These sensors will be used for perimeter defense, surveillance, target acquisition and



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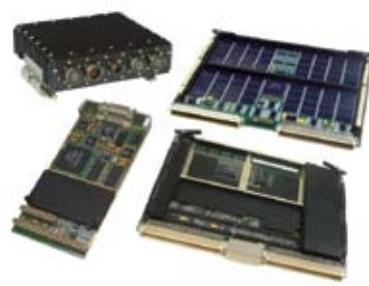
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As the speed and resolution of A/D and D/A data converters increase, the digital domain is being moved closer to the sensor, which is changing the signal processing architectures of data converters.



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situational awareness, including early warning of chemical, biological, radiological and nuclear threats. Fields of sensors will include a gateway node that exploits data synergies from suites of different sensor types, as well as long-haul communications abilities.

These complex data acquisition systems often include many widely distributed, high-speed sensors, whose data must be processed and fused in real time and made available simultaneously to all of the system's nodes. For example, image fusion applications merge images from multiple sensors operating in different wavebands to produce a fused image that contains far more information than a single camera could provide. The soldier can then quickly and efficiently identify regions of interest.

Sensors are also being deployed in the Future Force Warrior Advanced Technology Demonstration at the U.S. Army Natick Soldier Center. Here, much of the effort is directed toward physical protection, such as headgear with displays that allow information from multiple sensors, or images such as maps and messages, to be viewed.

Some simpler, low-end sensors are being used for measuring temperature, weight, displacement and light. Others are being deployed in weapons auto-loaders, while wireless acoustic sensors combined with onboard DSPs can detect fine distinctions in spoken language, engine vehicle noise and small arms fire. Radio frequency identification (RFID) sensors are even being used for logistics management and material inventory and control.

Finally, as the speed and resolution of A/D and D/A data converters increase, the digital domain is being moved closer to the sensor, which is changing the signal processing architectures of data converters. Alternatives include moving the DSP hardware closer to the sensor, or moving the data faster. Sometimes both methods are combined. In some systems, the data is being pre-processed to ensure that only the data of interest must be fully processed. ■



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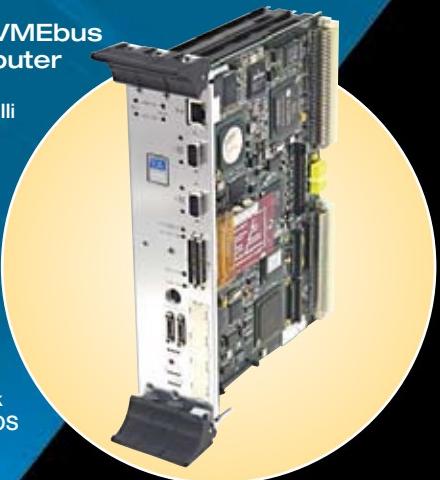
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Sensors in the Military

Acquiring Data Using New Sensor Technologies

Today's military data acquisition and precision machine control applications demand faster microprocessors, better performance and higher memory and packaging densities. In response, intelligent control subsystems are utilizing sophisticated sensors, or integrated suites of sensors, for manned and unmanned applications.

Doug Patterson, Aitech Defense Systems

Sensors are normally components of larger electronic subsystems, such as computer control and measurement systems. Analog sensors usually produce a voltage or current proportional to the measured quantity. The analog value is then converted to digital form with an A/D converter before the CPU processes it. Digital sensors provide a binary representation through serial communication to return information directly to the controller or computer.

Complex, active environments can demand varying levels of situational awareness, sometimes requiring multiple, concurrent detection of threats, coupled with personnel identification such as blue or red, friend or foe and terrain mapping. When multiple, different sensor types are combined into integrated suites, and the information is additive or complementary, these suites of sensors may employ "sensor fusion." This fusion simultaneously exploits the synergies of data from the different sensor types. These suites of sensors are becoming more intelligent for use in higher-end manned and unmanned applications.



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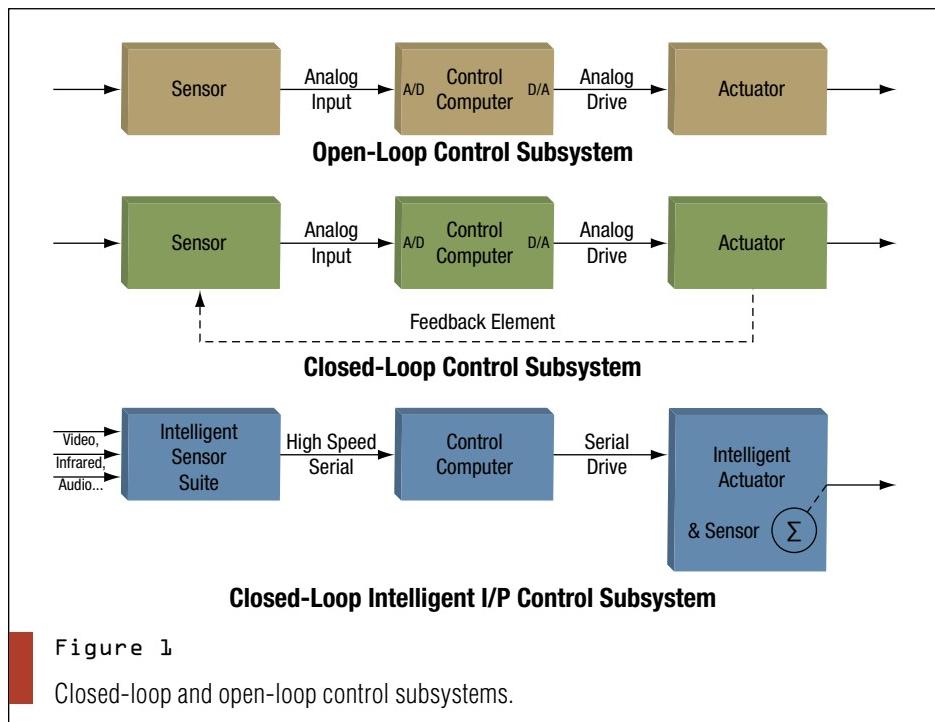


Figure 1

Closed-loop and open-loop control subsystems.

As with most sensor fusion applications, in many military applications acquiring data from more than one sensor, there is only one element that impacts a complex subsystem's architecture. Sensor fusion systems must do more than just provide multiple camera ports on a data or mission processor. They must also register the data streams to each other, sometimes using a third data set as

a reference. For instance, image processing subsystems can register and associate both the infrared (IR) and visible images, and compare and correlate them to each other. These images can then be overlaid onto a stored image from a topographical digital image map database.

However, not all applications require this level of sophistication or the requisite increased costs. Relatively simple



Figure 2

Five-slot, 1/2 ATR-short VMEbus-based vehicle management computer.

closed-loop and open-loop machine control applications include spatial azimuth and elevation positioning, autoloaders, vehicle suspension auto-leveling, main and auxiliary heating and cooling units and power conditioning. Many of these can employ non-intelligent, relatively simple discrete sensors. Even RF-sensitive devices are being used today. Depending

on the amount of anticipated data and the sensor functionality, sensor-based, situational and/or environmentally aware subsystems can be partitioned into one of two main areas: those that require high-end, self-contained sensor suites or those that are best suited to low-end, discrete sensors.

Selecting the right sensors is critical to implementing any military control-based subsystem in which the key factors are accuracy, precision, the ability to meet the environmental range of the intended application and cost. Other considerations include how these subsystems are configured to utilize positional or data feedback to ensure proper operation.

Today, most of these subsystems employ closed-loop control and are formed of four basic elements: a sensor input device, a control/computational element, a motivator/output device and a feedback loop (Figure 1). Although usually more expensive, closed-loop subsystems are used where high precision, stability or operational criticality are paramount. Open-loop controlled subsystems can be less expensive to implement since they normally do not include a feedback element. The risk with open-loop subsys-

tems is that, without feedback, they can sometimes get out of sync during operation, with unpredictable results.

High-End, More Complex Sensor Applications

Examples of high-end, integrated sensors include IR arrays, high-resolution monochromatic or color video cameras, microwave gamma radiation arrays, synthetic aperture radar (SAR), light detection and ranging (LIDAR), Hall-effect magnetic sensors, high-bandwidth software defined radio (SDR) and global positioning systems (GPS).

A suite of sensors can contain one or more intelligent sensors integrated into a single defined package. These sensors, if correlated to each other, can represent a fusion of once disparate data, now tightly bound together into a physical model of that environment. Intelligent sensors detect and capture their own raw data, gather and pre-format this data within the sensor suite and transmit the formatted data via a high-speed link to the processor array for post processing.

The data link can be sent through a standardized parallel data bus—typically RACEWay, or SkyChannel—or serially via high-speed serial ports such as CameraLink (the LVDS version), Digital Video Interface (DVI) or Gigabit Ethernet. Because these sensor links tend to be dedicated point-to-point links from the sensor to the mission computer, latency and data collision delays are minimized or avoided completely, and the data can be processed within the mission processor in real time.

One high-end application for complex, integrated sensor suites is automated target recognition (ATR) (Figure 2). For example, an intelligent, anti-tank missile with a non-radiating, passive sensor suite is fired from remote rear echelon areas toward known areas of enemy (or “red”) engagement. The missile heads toward an area that is also occupied by friendly “blue” force vehicles, which are interspersed in and among the “red” enemy positions. The missile subsystem can use GPS and low-level flight and terrain-following algorithms to locate and loiter in the area, while using its onboard visual

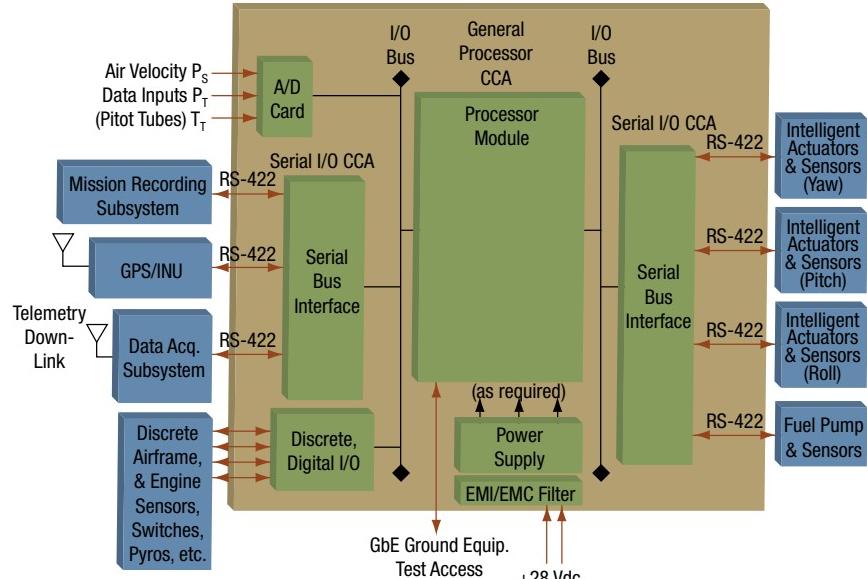


Figure 3

Typical autonomous UAV mission flight computer application.



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and IR cameras to sweep the specified area. It can rotate the captured visual and thermal images in 3D space, then analyze, correlate and compare the data to positively identify the “red” tank’s physical form from a stored visual and thermal attribute database. The subsystem can then take appropriate action without harming “blue” friendly forces.

Another high-end application is a self-contained LIDAR or SAR, where the data collected is pre-processed locally within the sensor. The data is then formatted and packetized, communication and data protocols are added, and the data is transmitted via a dedicated point-to-point high-speed serial (HSS) port or data fabric to the mission computer for post processing. For homeland security applications, an ultra-sophisticated sensor subsystem would include passive millimeter-wave radiometry for detection of concealed weapons and improvised explosive devices (IEDs). These subsystems detect the absorption of background “backscatter” microwave radiation. They can discern and identify differential densities of concealed potential threats, such as guns, knives and plastic explosives, from long “standoff” distances.

Simple, Low-End Sensor Applications

Low-end sensors include simple discrete mechanical and magnetic binary switches, thermocouples and thermistors, strain and pressure transducers, linear voltage displacement transducers (LVDTs), synchros and resolvers and photo-resistive and photo-voltaic cells.



Figure 4

Four-slot, 3U CompactPCI-based autonomous UAV mission computer.

The number of applications for low-end sensors is quite large, and includes motion and temperature limit detection, temperature measurement, weight, linear and rotary displacement measurement, and visible and non-visible light measurement.

A new area is the use of RF identification (RFID) devices for remote sensors. These are being used in the military today for material tracking,

inventory control and logistics management. RFIDs can be simple passive devices that take RF energy excitation from the detector to power the device, or they can be slightly more complex, active, integrated, battery-assisted devices that transmit their IDs and data when requested. As the cost of RFIDs drops, the use of these types of devices is likely to spread more widely. They may some day

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be used to track troop movement and even assist in battle management.

One example of a low-end sensor application is a weapons platform auto-loader. This platform subsystem controller employs mechanical or Hall-effect limit switches, absolute and relative position rotary encoders, angular and linear displacement and pressure transducers. These discrete sensors feed their

data into various analog and digital ports of the controller and ensure that rounds are quickly and accurately handled. They also ensure that rounds are properly and safely loaded into the breech or handled quickly, efficiently and safely during round replenishing. The controller can also store rounds in canisters and use RFIDs to ensure that rounds are properly manifested, tracked and inventoried.

Wireless, intelligent, acoustic sensors can be dropped or deployed into an area of interest. Onboard DSP processors can continuously monitor the area, checking for language dialects of conversations, engine noise from specific vehicle types, troop movements and small arms fire. The processors can transmit an encrypted warning and position to "blue" forces only when such specific acoustic signatures are recognized.

The flight computer of a fully autonomous unmanned aerial vehicle (UAV) is another application that can use simple actuators and discrete sensors to control the vehicle's takeoff, flight path, enemy engagement and landing (Figure 3). As the mission computers and sensor suites on these vehicles become more capable, their missions can become more complex and far ranging by providing greater levels of usable intelligence. They can even be used to engage enemy positions and be equipped with onboard, self-deployed threat countermeasures (Figure 4).

By incorporating additional processing and data sharing capabilities, sensors are adapting to meet the growing demands of military data acquisition applications. Both the more complex environments, and those that do not require intricate levels of data processing, are benefiting from these advancements in sensor technology. ■■

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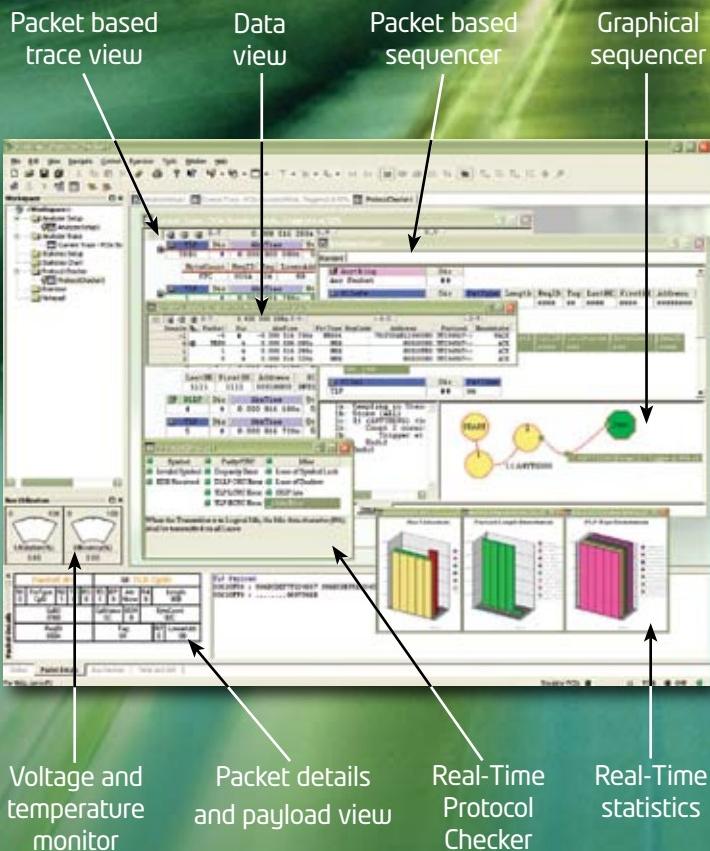
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Sensors in the Military

Data Converters and DSPs Getting Closer to Sensors

As the data converters used in military applications must operate faster and at greater resolution, the digital domain is moving closer to the antenna/sensor array. In response, two different approaches to DSP architectures are being used, sometimes in combination: moving the data faster, and/or moving the DSP hardware.

Scott Hames, Interactive Circuits & Systems
Part of Radstone Embedded Computing

The data converters used in military applications, such as defense communications and radar systems, must operate at ever-increasing speeds and higher resolutions. As a result, the digital domain is encroaching on the antenna or sensor array. As this happens, military system designers face serious challenges when trying to move signal data in ever-increasing volumes.

This situation is driving two different approaches to DSP architectures. One approach is to employ the latest innovations in bus technology to increase the speed/bandwidth of data movement, that is, moving the data faster. The other is to move some or all of the DSP hardware toward the source of the data, a "point of load" approach; that is, moving the data processing. The two techniques are not mutually exclusive and some systems will require both.

Moving the Data Faster

System architectures based on traditional back-end DSP and front-end A/D and/or D/A converters can still be effective in many situations, as long as the

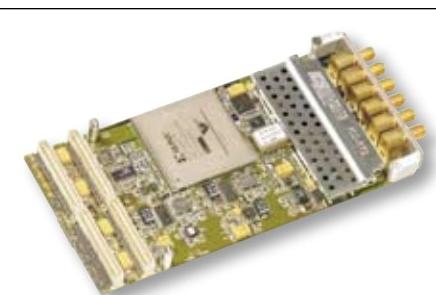


Figure 1

One approach to the faster speeds and higher resolutions in military data converters is moving some or all of the DSP hardware toward the source of the data. The latest generation of A/D and D/A converter modules, such as the ICS-572 from Interactive Circuits & Systems, features FPGA technology for pre-processing.

ability to move the data among processing elements is at an appropriately high level. The evolution of the PCI bus is a prime example of this.

But there are caveats to using a shared bus, such as PCI, as the backbone of a data acquisition system, especially when it is built up from off-the-shelf components such as bridges, switches and endpoints. The PCI endpoint, or local bus interface, can often make or break the performance of a data acquisition system. Bus masters

must balance the need to stream data at high rates for long durations, essential to efficient throughput, with the need to share the bus among multiple users. This usually means having the ability to disable arbitration schemes when the need for maximum throughput arises.

Unfortunately, most PCI master devices seem to be designed either for maximum throughput or for fair arbitration, but not both. Arbitration among multiple bus users can substantially reduce the aggregate bandwidth from the theoretical maximums, usually by artificially limiting the amount of time any single user can hold the bus. Valuable bus cycles are then wasted on multiple bus requests and retries.

A brute force solution to the need for guaranteed PCI bandwidth has been the implementation of multiple segment architectures, which provide more data buses between nodes such as data producers, data consumers and processing engines. Often, the number of processing engines is increased as well.

There are limitations associated with increases in clock speed and bus width, and skew between data lines on a wide bus such as PCI can destroy timing margins. Because of this, it is now generally accepted that serial buses running at high speed will provide better throughput for future data acquisition systems.



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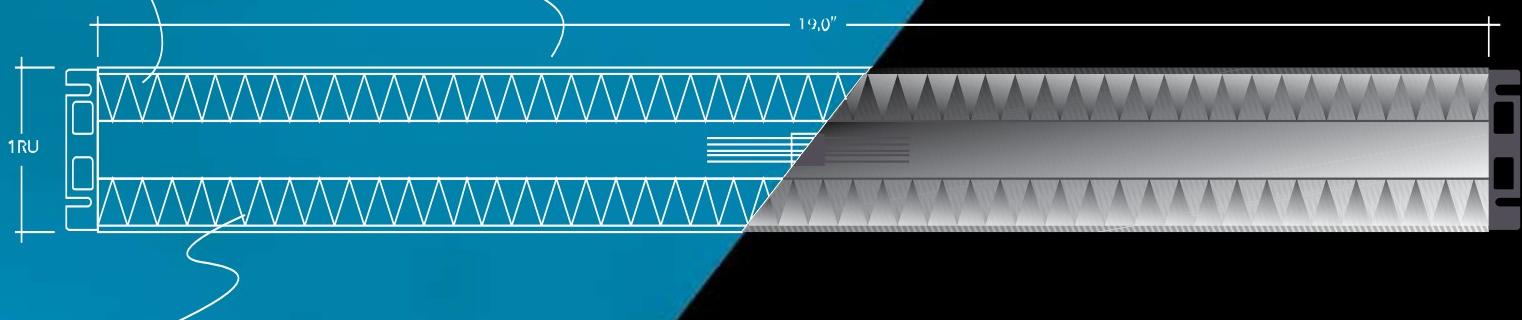
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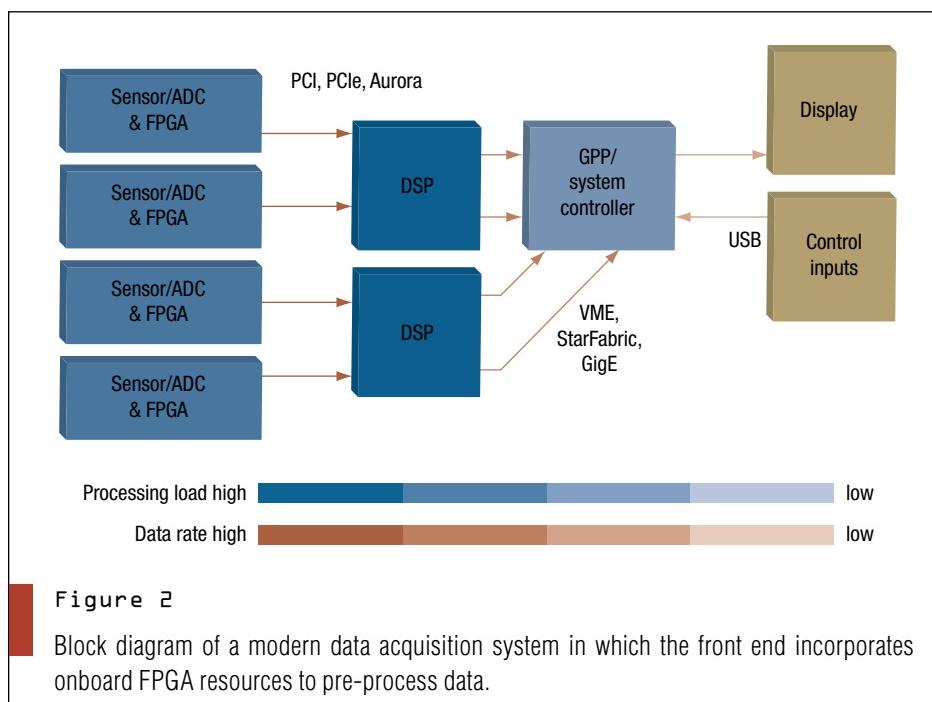


Figure 2

Block diagram of a modern data acquisition system in which the front end incorporates onboard FPGA resources to pre-process data.

Much of the PCI community is now in the midst of a migration to PCI Express. Despite the improvement over parallel PCI, this may not be sufficient for future high-speed data acquisition systems. Analog to digital converters now routinely exceed

1 GHz, and even if the resolution is only eight bits, a single channel will saturate a four-lane PCI Express link. Clearly, the strategy of moving large amounts of raw data has reached its limit, at least so far as today's available technology is concerned.

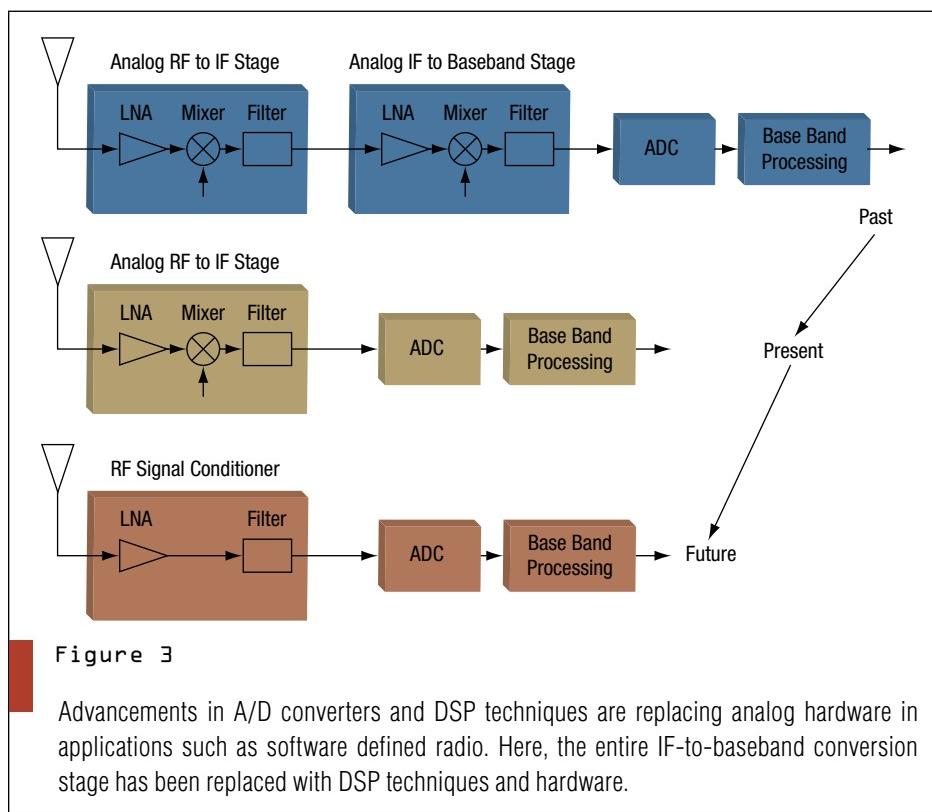


Figure 3

Advancements in A/D converters and DSP techniques are replacing analog hardware in applications such as software defined radio. Here, the entire IF-to-baseband conversion stage has been replaced with DSP techniques and hardware.

Moving the DSP Hardware

Given that, over time, the converters have moved closer to the sensor, why shouldn't the DSP hardware, or at least some of it, do the same? There are real opportunities for "point of acquisition" DSP hardware to extract the meaningful data from the extraneous data before moving it to a separate module for processing. In recent years, FPGAs have emerged as the de facto standard for custom hardware (Figure 1).

Most of the recently introduced data acquisition modules (Figure 2) feature some kind of onboard processing resource, either an ASIC or an FPGA. Combined with the adoption of high-speed serial bus technologies such as those previously discussed, these modules have allowed the creation of a new architecture for sensor processing systems, one that changes the meaning of the term "embedded processing."

One effect of the implementation of higher-speed A/D and D/A converter components is that the digital processing domain now encompasses operations that were previously executed using analog components and techniques. This is especially true of software defined radio applications, where the entire IF-to-baseband conversion stage has been replaced with DSP techniques and hardware (Figure 3).

Isolating Signals of Interest

A key technique for reducing the data rate is to focus on the signals of interest and eliminate redundant data. Many applications—including radar, communications and high-frequency sonar—use carrier frequencies much higher than the actual bandwidths of interest. If the band of interest can be shifted to a lower carrier frequency, ideally all the way to DC, the data rate required to represent the signals digitally can be reduced substantially, regardless of the techniques used to downconvert the signal.

The Nyquist sampling theorem states that the data rate required to represent the signal is twice the highest frequency of interest. A 100 kHz band located on a 70 MHz carrier requires a data rate of about 140.1 MHz to meet the Nyquist criteria, but the same 100 kHz band requires

only a 200 KHz data rate if it is located at baseband (DC) (Figure 4).

Until the introduction of high-speed, high-resolution A/D converters, band-shifting functions such as downconversion were done using analog components. But there are huge benefits to performing operations such as downconversion, or band shifting, using digital techniques. Even the best analog components add noise to signals. Compared to their analog counterparts, digital circuitry such as numerically controlled oscillators (NCOs) provide an unmatched combination of stability and flexibility. In addition, where digital processing techniques can allow exact execution of mathematical functions, analog circuitry often provides the closest approximation of a transfer function rather than what was actually required.

Design Considerations

Despite these benefits, serious risks exist when moving the boundaries of the digital domain in this manner. When

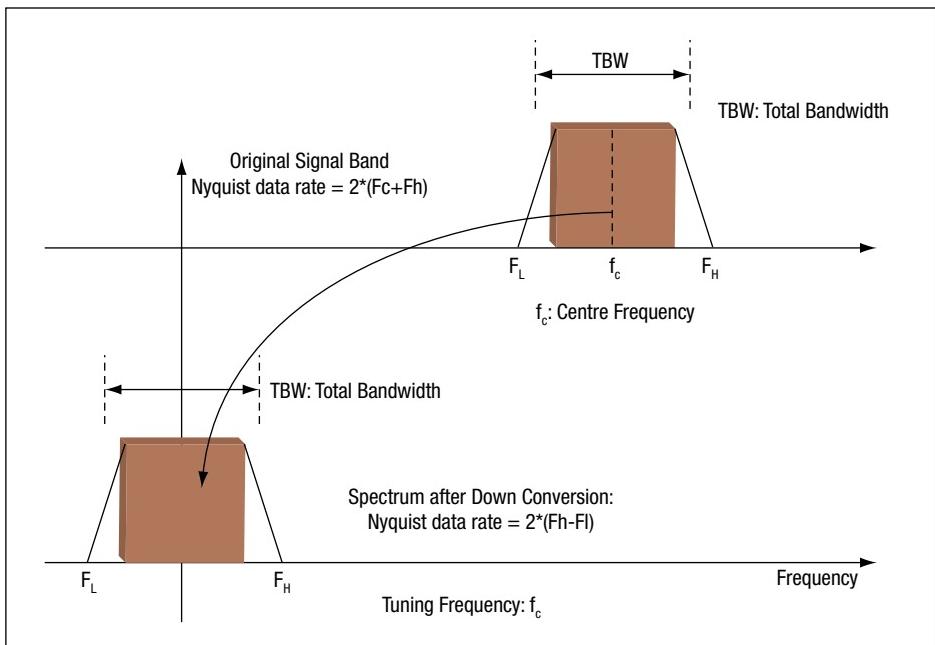


Figure 4

In some defense applications such as radar and high-frequency sonar, which use carrier frequencies higher than the actual bandwidths of interest, band-shifting techniques allow reduced data rates.

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replacing analog hardware with a DSP technique, it is imperative that the operation of the analog circuitry be understood exactly, and that the DSP hardware and techniques replacing the analog circuitry provide identical functionality.

This is particularly true of band shifting operations such as upconversion and downconversion. Careful application of DSP hardware—general-purpose, FPGA and ASIC—can greatly reduce the amount of data to be moved back to a host processor. But, despite its appeal, this approach requires careful component selection to ensure that the desired DSP functionality can be properly executed at the converter I/Os. Multi-channel and multi-event synchronized applications have special requirements that must be respected in order to make this approach work.

Digital upconversion algorithms are excellent examples of the need for proper execution in hardware. There are many interpolating D/A converters on the market that offer extremely high conversion rates and reasonable data input rates. However,

these may lack the ability to properly phase synchronize multiple events—an absolute prerequisite for pulsed operations such as coherent radar—or multiple channels, required for phase-sensitive operations such as beamforming. Mistakes in component selection can prevent proper system operation, even if the DSP algorithm is well thought out and carefully designed.

Digital downconversion (DDC) applications often have an extra requirement as well: the need to phase lock, or “track,” an incoming signal for the purposes of carrier recovery. Real-time adjustments to the NCO operation will be required to fine-tune the operating frequency so it exactly matches that of the asynchronous transmit system. This will usually require the DDC to be implemented in an FPGA, which will allow the designer to optimize the NCO performance for the target system.

The need to process rapidly increasing amounts of sensor-captured data is at a level that stretches the capabilities of the most sophisticated hardware. One

approach is to try to move the data faster, but theoretical speeds are not always achievable in practice. An alternative, or complementary approach is to pre-process the data, identifying and isolating only data that is of interest and discarding the remainder, which results in a potentially significant reduction in the amount of data to be moved. Whichever approach is followed, there are a number of factors to be taken into account in the design of the solution. However, if the tradeoffs are appropriately made and their implications precisely understood, solutions can be designed that will deliver the required levels of performance. ■

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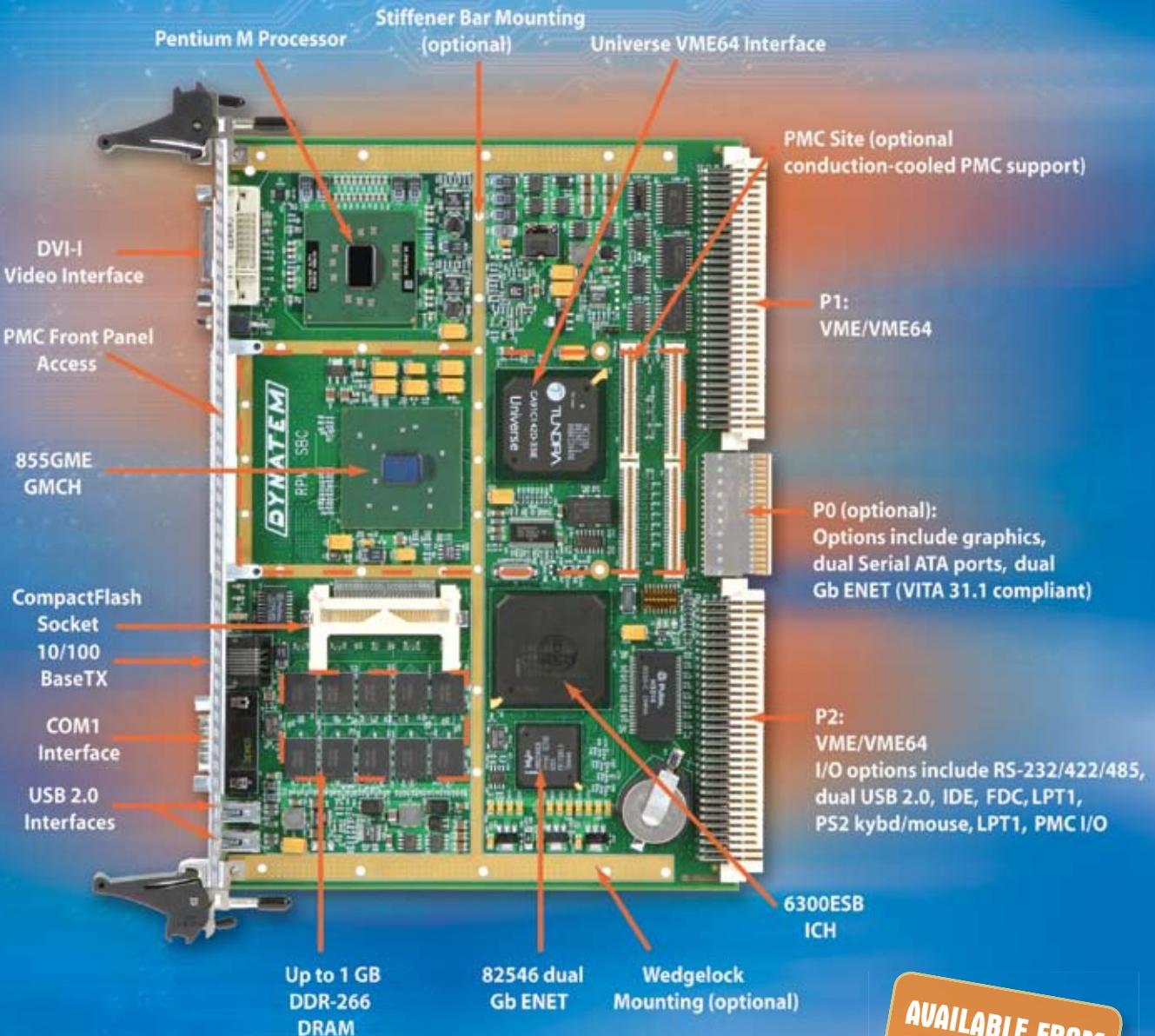


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Safety-Critical Software Standards

MILS: High-Assurance Security at Affordable Costs

Without Multiple Independent Levels of Security (MILS), integrators have to implement each level of security function individually on a separate processor. The MILS architecture on a single processor is both cost-effective and possible with today's technology.

Joe Jacob, Vice President
Objective Interface Systems

Over the past five years market forces have coalesced to support a dramatically simpler foundational architecture, called "MILS," for building high-assurance systems that must survive high-threat environments. Multiple Independent Levels of Security (MILS) is a departure from operating system architectures that were designed prior to the Internet, when there was little threat of network attacks. As a result, these early systems did not incorporate security as a design requirement. In response to inevitable failures and intrusions, patches were developed over time to plug specific security holes. This "fail first, patch later" approach is unacceptable for any mission-critical system.

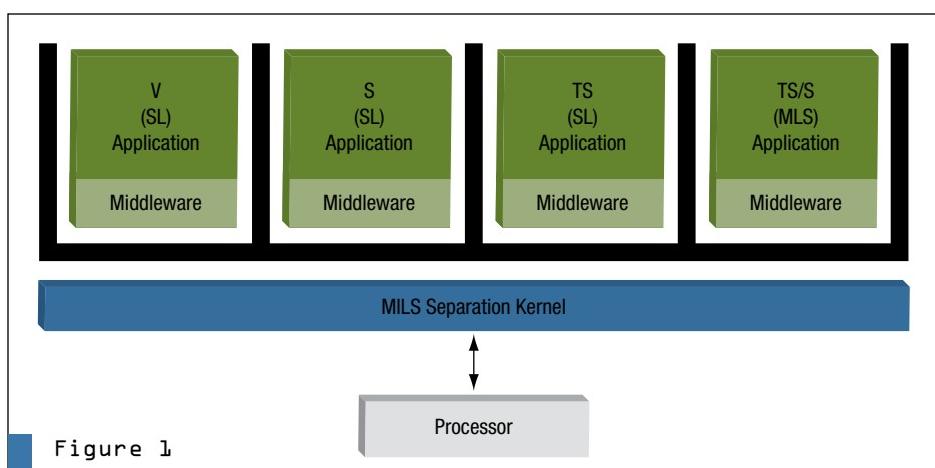
The central idea behind MILS is to partition a system in such a way that: 1) the failure or corruption of any single partition cannot affect any other part of the system or network, or, 2) each partition can be security-evaluated and certified separately, so no partition requires

evaluation at a higher level than necessary for that function. For the first time, developers can base their applications on secure, high-assurance foundations.

Multiple Levels of Security for Multifunctional Systems

In the early 1980s, the DoD issued the "Orange Book," a set of criteria used for evaluating the security features of computer systems. It became widely used in the IT industry as a benchmark for security standards. However, Orange Book security fell short in two areas. First, higher assurance

levels required both mathematical verification of trusted system components, as well as significant security functionality in those trusted system components. The code size made mathematical verification almost impossible. Secondly, intersystem communication was not addressed by the Orange Book. Trusted components and device drivers ran in privileged mode for performance reasons. Security-critical application code also ran in privileged mode. This was a nightmare to evaluate, and typical evaluations cost on the order of \$100 million.



This basic architecture diagram of MILS, shows it divided into three layers: separation kernel; middleware, including the Partitioning Communications System (PCS); and applications.



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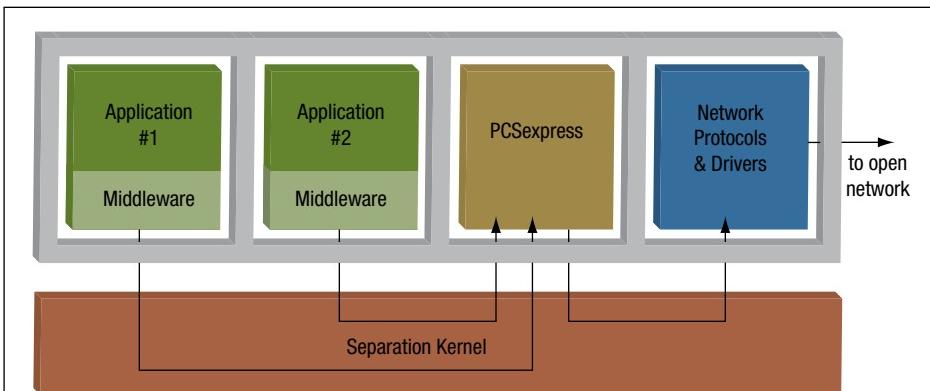


Figure 2

When a distributed system configuration is created, the goal is to make it as safe or secure as if it were just a single processor. That's accomplished by implementing end-to-end enforcement of the basic MILS separation kernel policies. The Partitioning Communications System (PCS) is the enforcement mechanism. The collection of MILS nodes in a distributed system is called an enclave, and the PCS is present in each node in the enclave. The PCS fits between the applications and the partitions implementing network protocols.

As a result, implementing Orange Book standards became expensive and problematic, mainly because of the limitations of microprocessors in the 1980s. The tremendous increase in microprocessor performance has enabled new paradigms of security. Often, one system has the job of performing several different functions, especially as processors increase in performance. If such a multifunctional system must meet different levels of safety or security criteria for each of its functions, there must be some guarantee that lower-security functions cannot interfere with higher-level functions—under any circumstances.

Such systems require Multiple Independent Levels of Security, or MILS, as the NSA designates them. MILS system designers must guarantee that unintended interactions are not possible. Otherwise, systems integrators would have to integrate each function individually on a separate processor, which would increase costs and system complexity. In some applications, such as fighter aircraft, separate processors would also add weight, take up space, and consume power—a serious design drawback. MILS implementation on a single processor is both cost-effective and possible with today's technology. MILS is not a

revolution of new ideas over old, but old ideas coming of age—now that technology has caught up.

One Size Does Not Fit All

MILS combines the best of the safety and security worlds to create a better solution than either could have devised alone. It draws upon FAA DO-178B Level A Safety technology and Common Criteria EAL7 Security technology to enable MILS Web and network services for mission-critical embedded and real-time systems, including high-assurance weapons, training and communications systems and C4I platforms.

MILS is founded on the understanding that security is not a one-size-fits-all proposition, and that the security level should be appropriate to the application. The Common Criteria's Evaluation Assurance Levels range from EAL1, the very basic level, to EAL7, the highest level of assurance. Various military systems require EAL assurance levels according to the value of their data and the threat that they encounter. A set of assurance requirements between EAL6 and EAL7, called "High Robustness," is required when top secret, secret, confidential and unclassified data reside on the same node.

Military command centers derive information from a variety of sources, from weather forecasting systems to fighter jets to commanders and allied forces in the field. Users within intelligence agencies and the DoD wrestle with information on multiple computers handling information at varying security levels.

An operating system that can simultaneously support ubiquitous commercial applications running on Windows or Linux, along with a variety of mission-critical or high-assurance applications, is the holy grail of computing. Without such a capability, system designers need to use multiple hardware devices to meet varying security requirements. This type of hardware separation is costly and awkward. An architecture that can support secure partitioning, commercial or legacy applications, multilevel communication, secure user authentication and trusted path, and secure cross-domain information transfer—in a single processor—is the promise of MILS.

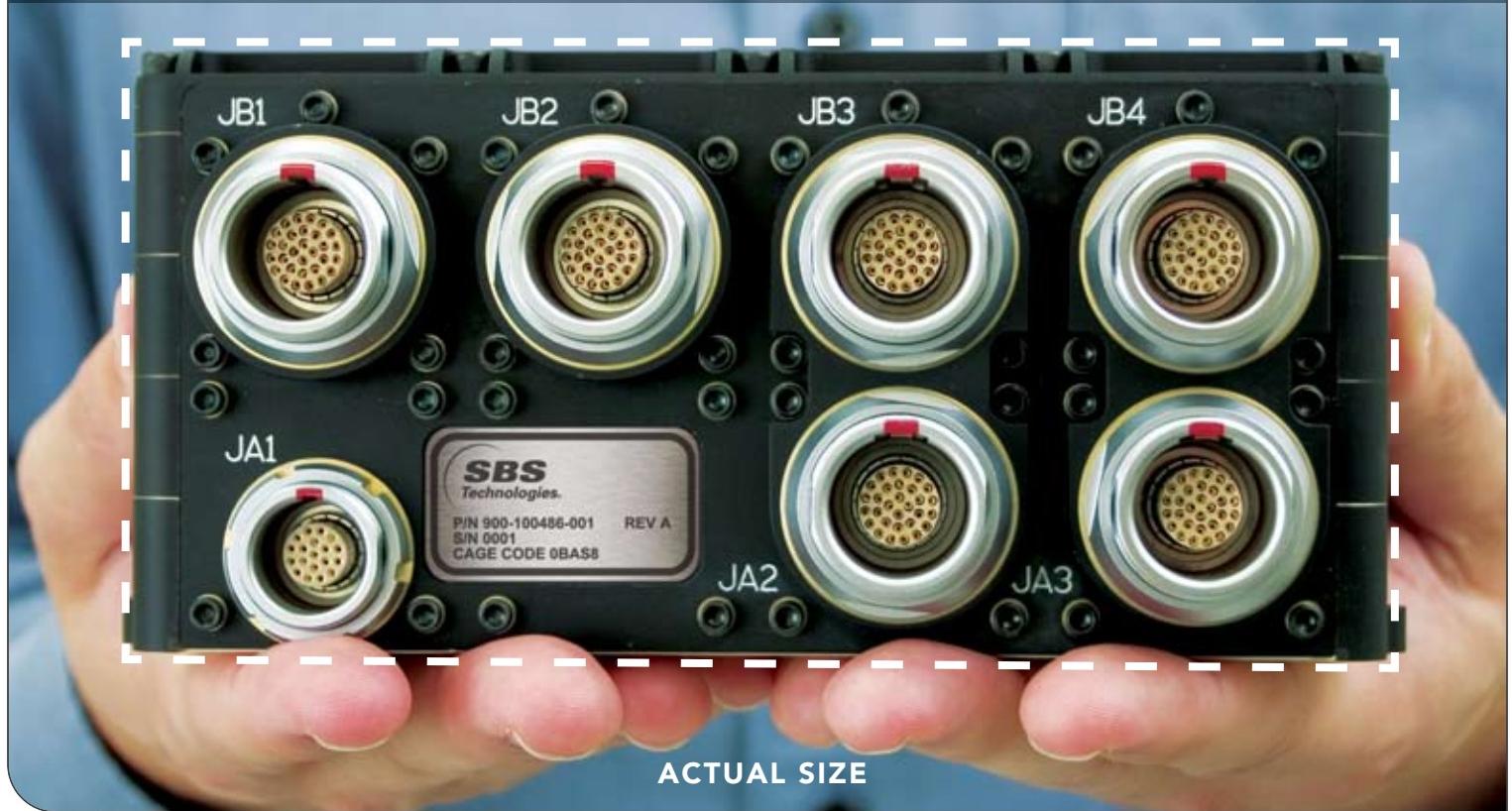
Minimum Code Equals Affordable Cost

MILS architecture separates security mechanisms into manageable components. Processes are isolated into partitions that comprise a collection of data objects, code and system resources. These individual partitions can be evaluated separately. This approach substantially reduces the proof effort for secure systems.

To support these partitions, the MILS architecture is divided into three layers: separation kernel; middleware, including the Partitioning Communications System (PCS); and applications. Figure 1 is a basic architecture diagram of MILS. While those terms have been used since the days of the PDP-11, what is different is the assignment of functions to these layers.

Separation Kernel. The MILS separation kernel divides the computer into separate address spaces and scheduling intervals, guarantees isolation of the partitions and supports carefully controlled communications among them. Because the separation kernel performs these functions and only these func-

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tions, the source code can be small—roughly 4,000 lines of C language code. This makes it fast and practical to verify using formal analysis methods (mathematical verification) and to do the exhaustive testing and comprehensive documentation required for the highest-level certifications. The separation kernel requires the highest level of authentication, and is the only piece of software that runs in privileged mode. Therefore, no other code, not even device drivers, has the ability to affect the processor's protection mechanisms. Everything else, including all middleware, runs in user mode. The small size of the separation kernel is a manifestation of the most important MILS design objective. It is because of this rigorous inspection and evaluation that the MILS separation kernel can be trusted.

Middleware. In the MILS architecture, middleware has a broader meaning than just traditional middleware. Most of the traditional operating system functions have been moved from the operating system to “middleware ser-

vices,” e.g., file systems, device drivers, trusted path, etc. Middleware services include a Partitioning Communications System (PCS) to extend the scope of the separation kernel to intersystem communication. It also includes traditional middleware like CORBA (Common Object Request Broker Architecture), DDS (Data Distribution Service) and Web services. Middleware resides in the same kind of partition as the application that it supports, either co-resident with the application or in a partition by itself. Middleware runs in unprivileged (user) mode, making these services subject to separation kernel policy enforcement. The services that previously ran in privileged mode as part of the operating system, such as memory allocation, device drivers, I/O primitives, file systems and network stacks, now run in user mode in the MILS middleware layer. Some middleware components don't need to be certified at the highest level, and because they can be confined to one partition, they can be evaluated and certified at the appropriate level at much less cost.

For example, if a component such as real-time CORBA is running in a classified partition and another instance of it is running in an unclassified partition, only the classified instance of CORBA needs to be certified.

Applications. The application level entities manage, control and enforce their own application-level security policies, such as firewalls, crypto services and guards. Instead of the “fail first, patch later” approach, trusted components are mathematically verified so that they are: Nonbypassable, Evaluatable, Always invoked and Tamperproof. Taken together, these form the acronym NEAT. In order to be effective, all system protection must be NEAT.

To satisfy the High Robustness requirements of EAL6/7, engineers must design the system with security in mind from the start and must make it possible to decompose every system function into successively smaller subsets, down to a simple, provable module, each step demonstrating that mechanisms are “NEAT.” This formal proof requires

Why MILS Is Important: A JTRS Example

Imagine a field commander in the most demanding security environment: a combat situation. He has secret information to share with allied commanders. He has top-secret communications to send to Central Command, and unclassified information to send to soldiers in the field.

Radio often provides the only means of communication in high-risk military environments. Unfortunately, military personnel have been unable to trust that radios will be effective at separating multiple levels of classified and unclassified transmissions. They need to know that secret communications on one channel intended for U.S. forces only (classified as “NOFORN” or not foreign) won't bleed into unclassified channels, or be intercepted by hostile third parties.

Further complicating the matter is the wide number of incompatible devices in the field, including aging legacy technology. Ensuring interoperability among different types of field-based radios operating at different frequencies is mission-critical.

Until recently, manual separation of classified messages and hand delivery have been the only secure options available. Now, however, the Joint Tactical Radio System (JTRS) has been initiated by the Department of Defense to provide a flexible new approach to meet diverse warfighter com-

munications needs—through high-assurance software programmable radio technology, or software defined radio (SDR).

MILS is a perfect match for the JTRS because it ensures a high level of security while enabling modularity of new capabilities, scalability of bandwidth and channels, and backward compatibility with legacy radios. It also supports the dynamic intra- and inter-network routing of data transport that is transparent to the radio operator.

Objective Interface Systems views MILS as the secure foundation to protect and enable real-time CORBA-based SDR systems—initially for building the most effective, secure software-based radio system possible for mil/aero use, to make JTRS radios secure conduits of multilevel, multichannel communication, and later for providing flexible and secure wireless communications for the commercial markets. As an active member of the OMG, Objective Interface is leading the development of a real-time and MILS-compliant profile for CORBA. Objective Interface's ORBexpress middleware solution offers a commercially available SDR platform that enables interoperability through software modifications, not hardware changes. As a result, future software radios will be interoperable much like the international phone system.

Systems Are Vulnerable to Many Kinds of Attacks	
Bypass	An attacker uses a flaw in a security system to circumvent security mechanisms to get system or network access. The actual point of entry is through either a hardware device or a program that enables the user to access the system without going through security clearance procedures such as authentication. A bypass may be put in place by an attacker, or it may be a design flaw, or even a diagnostic facility accidentally left in place by developers.
Compromise	An invading program reads private data. An example is spyware. If invasive software can monitor the data of programs running on the system then security has been breached.
Tamper	An attack that makes unauthorized modifications to data or program code. If tampering is possible then no application is safe from viruses and worms.
Cascade	Malicious users or software cause failures to cascade from one system component to another. If the failure of one application can cause another application to fail, then it may be possible to bring down the whole system.
Covert Channel	Information is leaked to an unauthorized recipient through a communication channel that is accidental or unintended. By detecting the presence or absence of a message, for example, an unauthorized observer can derive information about the activity of the communicating parties.
Virus	Malicious software invades privileged functions to infect all parts of the system and spread to other connected systems.
Subversion	Malicious software is innocently loaded into the system by an authorized user who mistakenly believes the software is legitimate

Table 1

MILS enables protection against malicious software, internal mistakes and failure. Malicious software can successfully attack the system's hardware or software foundations and render any form of security useless. Security "patches" that do not address security at the foundation level are vulnerable to a variety of forms of attack, as shown in this table.

extensive analysis, documentation and review. It is economically infeasible to achieve High Robustness unless the system is designed from the inception to be "provable." This cannot be added on after the fact.

When a distributed system configuration is created, we would like it to be as safe or secure as if it were just a single processor. That's accomplished by implementing end-to-end enforcement of the basic MILS separation kernel policies. The Partitioning Communications System (PCS) is the enforcement mechanism. The collection of MILS nodes in a distributed system is called an enclave, and the PCS is present in each node in the enclave. The PCS (Figure 2) fits between the applications and the partitions implementing network protocols.

The secure separation kernels developed by companies such as Green Hills, Wind River and LynuxWorks provides the ability to separate multiple address spaces. In one millisecond, the system may perform a safety-critical task, the next millisecond, not; the non-safety-

critical and safety-critical won't interfere with each other.

The separation kernel is microprocessor-centric. On this microprocessor, one can build a firewall that separates applications—top-secret from not, safety-critical from not—and guarantee that those applications won't talk to each other without an application-centric firewall. The separation kernel makes decisions about what goes on at the microprocessor level, but it knows nothing of the network. It just secures this one node.

The PCS takes this secure environment in the separation kernel and extends it to an enclave of computers—2, 100 or 10,000 computers. There will still be an application-centric firewall that separates applications, but it must be NEAT. Partitions are no longer restricted to being on the same processor. There could be hundreds of microprocessors, but one can still guarantee the firewall is tamperproof and nonbypassable. The MILS architecture makes it possible to secure tens of thousands of computers in a global information

grid—on fighter aircraft, tanks, aircraft carriers and destroyers.

MILS enables protection against malicious software, internal mistakes and failure. Malicious software can successfully attack the system's hardware or software foundations and render any form of security useless. Security "patches" that do not address security at the foundation level are vulnerable to a variety of forms of attack, as shown in Table 1.

Simple Means Secure

Past efforts at making software truly secure usually added complexity and high cost. Layers of protection were added on top of the operating systems, middleware and applications. Sometimes these layers interfered with each other, had unintended side affects or were not completely consistent with each other, giving both bugs and attackers the initial crack in the wall they needed to inflict damage.

The MILS approach is precisely the opposite. Systems are made more secure by making the protection simpler. Because it is simpler, it can be trusted to work under all conditions. The processor, via the MILS separation kernel, is tightly controlled. All protections built into the system will be composable—that is, the components will work the way they were designed to work and information will flow between them only the way that it should. The PCS provides the same assurances for distributed systems.

In collaboration with its partners, including the U.S. National Security Agency, U.S. Air Force Research Laboratory, the University of Idaho, Lockheed Martin, Raytheon, Boeing and Rockwell Collins, Objective Interface is working to integrate several MILS security separation kernels with Objective Interface's high-performance implementation of the PCS architecture, PCSexpress. Objective Interface is developing PCSexpress as well as real-time MILS versions of its signature products, ORBexpress and DDSexpress.

The MILS Separation Kernel Protection Profile (SKPP) is under final review by members of The Open Group. Once

The Softer Side

evaluated and endorsed by The Open Group, the SKPP will be officially evaluated and endorsed by the National Information Assurance Partnership (NIAP) as a validated protection profile, probably during the end of 2005. Developers can use the draft SKPP to plan MILS-based systems. The draft is available for download from www.niap.nist.gov/pp/draft_pps.

The MILS architecture is being applied today and will continue to be important in the most demanding applications where failure is unthinkable: airborne software and national security systems. Because it is both secure and affordable, it will be practical to use this architecture in commercial applications and anywhere system failure or unauthorized access will have significant or even life-threatening consequences. For more information about MILS and current news of MILS developments, visit <http://mils.ois.com>. ■■

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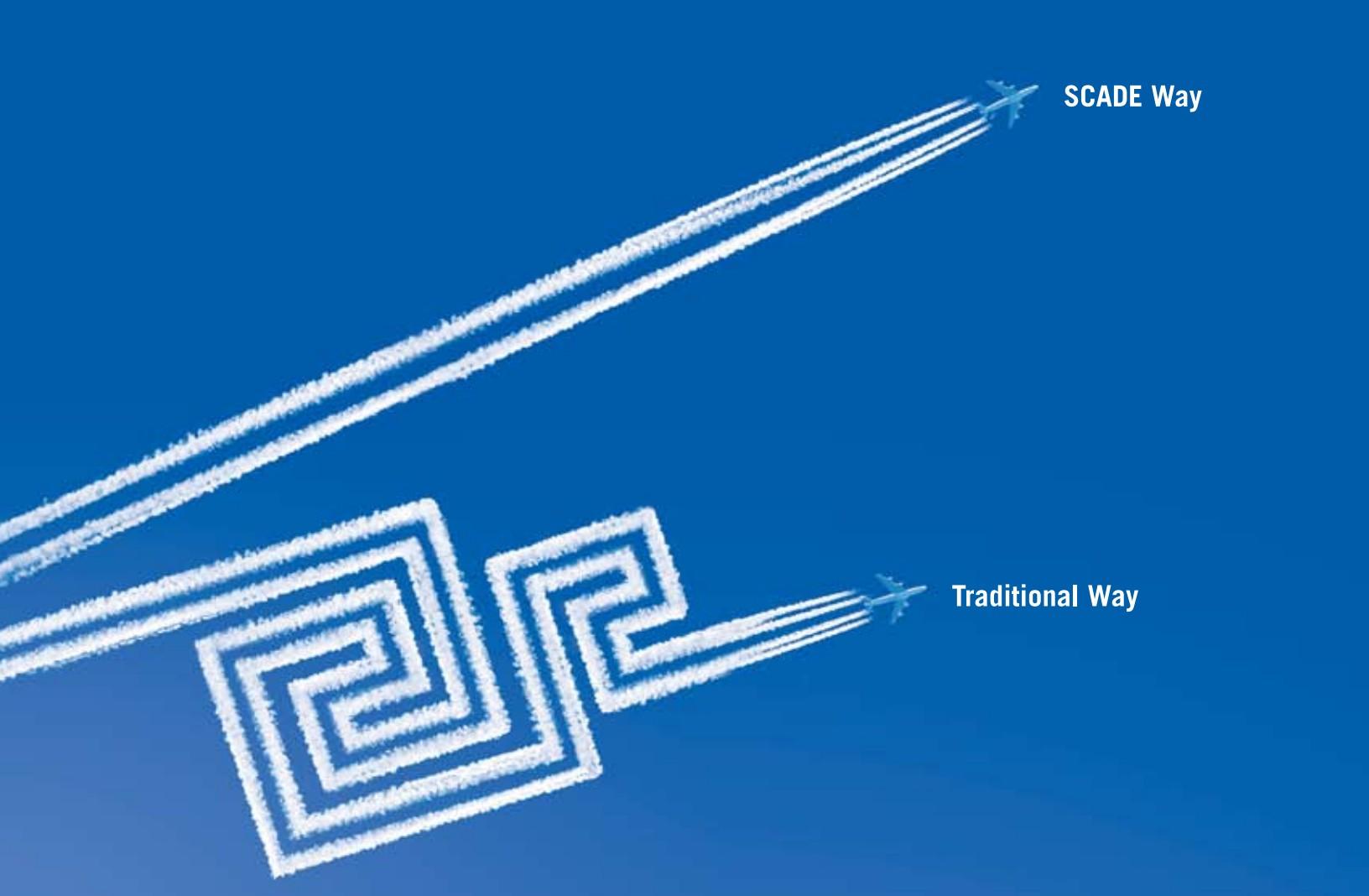
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On the Softer Side

Safety-Critical Software Standards

Ada 2005 Strengthens Ada's Safety-Critical Muscles

Ada boasts a respected legacy in safety-critical mil/aero apps. An emerging 2005 rev of the language improves on that legacy, while overshadowing the advantages offered by more modern programming languages.

Robert B. K. Dewar, President and CEO
AdaCore

Certain kinds of applications leave no margin for error. Software that flies an aircraft or that controls a nuclear reactor must work correctly, or the results could be catastrophic; such software is said to be safety-critical. Regulatory agencies in safety-critical domains typically have stringent certification requirements that must be met by software providers, beyond what would be standard practice for most military embedded systems. The goal is to provide assurance that the delivered system is reliable (it does what it is supposed to do) and is also safe (it does not do what it is not supposed to do).

For the development of safety-critical software, the choice of programming language makes a significant difference in meeting the requirements of exacting safety standards and, ultimately, high-reliability applications. Ada, for example, has a long history of success in the safety-critical domain. In a recent example, Ada was used in software for the mission control system (MCS) aboard Boeing's advanced aerial refueling tanker, the KC-767 (Figure 1).

The Italian Air Force was Boeing's

first KC-767 customer, ordering four of the world's newest and most advanced tankers, the first of which had its maiden flight this past May. The KC-767 MCS is the first avionics application in flight to use the Software Common Operating Environment (SCOPE), which consists of a safety-critical-certified ARINC653 operating system from Wind River, the GNAT Pro for VxWorks 653 Ada compilation system from AdaCore, and infrastructure software developed by Smiths Aerospace.

Well-Seasoned Language

Ada was designed from the start to promote sound software engineering, with features such as strong typing that help detect errors early. Ada's semantics are well defined and, unlike Java, the language has gone through a rigorous international standardization process that guarantees a thorough and detailed review. Ada also lacks the "traps and pitfalls" that cause run-time surprises in other languages, such as C and C++.

The Ada language was first introduced in 1983—the date of the first ANSI standardization. From the start there was a fundamental commitment to safety and reliability. Fitting that commitment, a formal process and an extensive test suite were introduced for testing an implementation's conformance with the language standard. This process has been known informally

as "validating" an implementation. Today that validation process is defined in an ISO (International Organization for Standardization) standard. Ada is the only language for which such a standardized set of conformance procedures exists.



Figure 1

Ada was used in software for the mission control system (MCS) aboard Boeing's advanced aerial refueling tanker, the KC-767. The Italian Air Force was Boeing's first KC-767 customer, ordering four of the world's newest and most advanced tankers, the first of which had its maiden flight this past May. The MCS's software environment consists of a safety-critical-certified ARINC653 operating system from Wind River, the GNAT Pro for VxWorks 653 Ada compilation system from AdaCore, and infrastructure software developed by Smiths Aerospace.



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In 1995, as a result of a significant effort sponsored by the U.S. DoD, a major revision of the language standard was published, popularly called Ada 95. Ada 95 brought a number of enhancements, including support for object-oriented programming, and became the first internationally standardized object oriented language. In accordance with Ada's fundamental design principles, key objectives were safety and reliability, and Ada 95's object-oriented features preserve this goal, while providing important capabilities such as inheritance with type extension.

No DoD Funding This Time Around

ISO procedures call for revising standardized languages every ten years. Although the DoD no longer requires specific languages, and thus did not fund the new

revision, major work was again invested, this time provided by the Ada vendor and user community, with some sponsorship by the Ada Resource Association (an industry trade group). The new proposed standard, which is referred to as Ada 2005, incorporates another decade of experience in using Ada to build large safety-critical systems, for example the onboard avionics control of the Boeing 777, and also a decade of research in language design.

The new language is not yet officially standardized, but the technical work is complete, and formal standardization is expected sometime next year. Meanwhile, Ada vendors are proceeding with its implementation, and Ada 2005-based products are available and in use today. There are important contributions that

the use of Ada 2005 can make in ensuring safety and security of large critical software applications.

It is interesting to note that the phrase "safety-critical" specifically applies to applications where human lives depend on correct operation—for example, commercial avionics. However, in a society increasingly dependent on sophisticated computer software, there are more and more applications where correctness is essential, even if they are not formally considered safety-critical. For example, the commercial banking structure relies on complex computer controls. Even a minor failure can cause waves that can have huge economic consequences. There are several decades of experience in building safety-critical systems, and the success has been remarkable—no fatalities can be attributed to failure of certified safety-critical software. It is both practical and essential to extend these techniques to improve the reliability of our entire computer infrastructure.

Ada 2005 Improves on Ada's Strengths

Ada 2005 brings a number of improvements to the Ada language. Some of the key enhancements are in the areas of object-oriented programming (OOP) interfaces, program packaging and an extensive containers library.

Ada 2005 extends Ada 95's OOP support to include the concept of interfaces. The interface feature of Ada 2005 is similar to that in Java, except that it is designed to have a more controllable and more static implementation where this is appropriate. One of the difficulties with OOP is that the notion of dynamic dispatching, which is central to the semantics of Java and typical C++ programs, is fundamentally at odds with the safety certification.

The problem is that dynamic dispatching is all about not knowing the flow of control and leaving this to run-time choice, whereas certification is all about knowing the flow of control statically so it can be analyzed and tested. Major work is in progress on resolving this conflict, but meanwhile an interesting and valuable approach is to use OOP techniques to take advantage of specializing and reusing standard libraries, but without using dynamic dispatch.

An important addition to Ada 2005 is the introduction of an extensive containers library. The design is somewhat similar to that of the C++ STL (standard template library), but it takes advantage of important recent advances in data structure research. It also exploits the strong features in Ada for generic programming, which have been considerably extended in Ada 2005, notably by adding the capability of partial parameterization, allowing partial specialization of reusable code. Unlike the templates in C++, where you cannot tell until you use them whether they are type safe, the corresponding generic features in Ada guarantee that a generic unit that compiles without error can be successfully instantiated without causing errors.

One of the great strengths of Ada from its inception was the package concept, which provides strict separation of specification from implementation (notably missing in Java, which combines specification and implementation in one syntactic unit, the class, and possible in C++ only by adopting extra lingual conventions). This was strengthened in Ada 95 by the addition of child libraries, allowing the structuring of code into a hierarchical set of components with strict control over visibility of encapsulated state data and methods.

In Ada 2005, the package mechanism has been extended (with the notion of "limited with") to allow this kind of separation and encapsulation, even in the presence of types that depend on one another, correcting a problem that had proved to be a restriction in usage previously.

Ada 2005: A Family of Languages

For purposes of developing safety-critical systems, Ada 2005 may be regarded not as a single language but rather a family of languages. In practice in writing high-reliability software, one does not want to use the full facilities of a complex language, since excessive complexity is an enemy of reliability. Instead a reliable subset is chosen.

All general-purpose languages use this subset approach, but two aspects make Ada unique. First, the notion of such subsets is built into the language standard, rather than being external to it (the latter is exemplified by the attempt to define a "safe C" subset such as MISRA C). Second, the specific features in the subset can be chosen by the application developer, thus providing a high degree of flexibility. Indeed, such flexibility is essential in practice, since the exact set of features in the subset depends on the analysis techniques that are expected to be used during the development process, which in turn depends on the level of criticality.

The concept of language-defined subset was introduced in Ada 95 in the form of a specific compiler directive, pragma Restrictions, and formalized and extended in Ada 2005. For example, in many kinds of safety-

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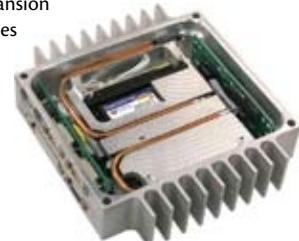
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Bus	AT Expansion Bus	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCI Universal Expansion Bus	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PC/104-Plus PCI Bus Masters	4	4	4	4	4	4	4	4	4	4	4	4	4	4
APIC (add'l PCI interrupts)	9	9	9	9										
CPU and BIOS	CPU Max Clock Rate (MHz)	650	650	650	650	1G	1G	1G	1G	333	333	333	333	100
ACPI 2.0 Power Mgmt	✓	✓	✓	✓	✓	✓	✓	✓						
Max Onboard DRAM (MB)	512	512	512	512	512	512	512	512	256	256	256	256	256	32
RTD Enhanced Flash BIOS	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Nonvolatile Configuration	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Quick Boot Option Installed	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Fail Safe Boot ROM (KB)	768	768	768	768	768	768	768	768	768	768	768	768	768	384
USB Boot	✓	✓	✓	✓	✓	✓	✓	✓						
Peripherals	Watchdog Timer & RTC	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
I/O	IDE and Floppy Controllers	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
SSD Sockets, 32 DIP	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Audio	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
TFT Panel TTL or LVDS														
SVGA Interface	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
AT Keyboard/Utility Port	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PS/2 Mouse	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
USB Mouse/Keyboard	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
I/O	RS-232/422/485 Ports	2	2	2	2	2	2	2	2	2	2	2	2	2
	USB Ports	2	2	2	2	2	2	2	2	2	2	2	2	2
10/100Base-T Ethernet	1	1	1	1	1	1	1	1						
ECP Parallel Port	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
aUDIO™ (Advanced Digital I/O)	18	18	18	18	18	18	18	18	18	18	18	18	18	27
multiPort™(aUDIO, ECP, FDC)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	
SW	ROM-DOS Installed	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
	DOS, Windows, Linux	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓



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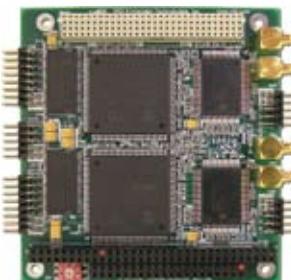
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Bus		AT Expansion Bus	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
PCI Expansion Bus Master			✓	✓	✓			✓	✓						
McBSP™ Serial Ports			✓	✓	✓			✓	✓						✓
Analog Input	Single-Ended Inputs	16	16	16	16	16	16	16	16						
	Differential Inputs	8	8	8	8	8	8	8	8						
Conversions	Max Throughput (kHz)	500	1250	1250	1250	500	100	1250	100						
	Max Resolution (bits)	12	12	12	12	12	16	12	16						
Digital I/O	Input Ranges/Gains	3/4	3/7	3/7	3/7	3/4	1/4	3/6	1/4						
	Autonomous SmartCal™ Data Marker Inputs	✓	✓	✓	✓	3	3	3	3						
Analogue Out	Channel-Gain Table	8k	8k	8k	8k	8k	8k	8k	8k						
	Scan/Burst/Multi-Burst	✓	✓	✓	✓	✓	✓	✓	✓						
Opto-Isolated	A/D FIFO Buffer	8k	8k	8k	8k	8k	8k	8k	8k						
	Sample Counter	✓	✓	✓	✓	✓	✓	✓	✓						
Relay Outputs	DMA or PCI Bus Master	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓				✓
	SyncBus	✓	✓	✓	✓			✓	✓						
Total Digital I/O	Total Digital I/O	16	16	16	16	16	16	16	16	16	48	32	64	32	48
	Bit Programmable I/O	8	8	8	8	8	8	8	8	8	24				48
Advanced Interrupts	Advanced Interrupts	2	2	2	2	2	2	2	2	2	2				2
	Input FIFO Buffer	8k	8k	8k	8k	8k	8k	8k	8k						2M
Opto-Isolated	Opto-Isolated Inputs											16	48	16	
	Opto-Isolated Outputs											16	16		
User Timer/Counters	User Timer/Counters	2	3	3	3	2	2	3	2	3	3				10
	External Trigger	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓				✓
Relay Outputs	Relay Outputs														16
	Analog Outputs	2	2	2	2	2	2	2	2	4					
Analog Out	Max Throughput (kHz)	200	200	200	200	200	100	200	100	200					
	Resolution (bits)	12	12	12	12	12	16	12	16	12					12
D/A FIFO Buffer	Output Ranges	3	4	4	4	3	1	4	1	4					
	D/A FIFO Buffer		8k	8k	8k		8k		8k						

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critical applications it is inappropriate to use dynamic memory allocation, because of the possible resulting unpredictability of memory usage. By specifying pragma Restrictions (No_Dynamic_Allocation), the programmer has effectively specified a language subset. Any attempt to use dynamic allocation will be flagged as a compile-time error. And importantly, the implementation can exclude from the executable any runtime support for dynamic allocation, thus simplifying the certification process.

Ravenscar Profile

As another example, the use of the full Ada concurrency model has long been regarded as inappropriate for safety-critical applications. A 1997 international workshop on real-time Ada issues defined a set of tasking features, named the Ravenscar profile, simple enough to be efficiently implementable and amenable to certification, yet powerful enough for the needs of realistic applications. The Ravenscar profile is defined by a set of restrictions such as no locally declared tasks, no dynamic allocation of tasks and no asynchronous transfer of control.

A program conforming to the Ravenscar profile comprises a fixed number of tasks where each task body is an infinite loop with a single “invocation event” at each iteration (Figure 2a and 2b). The invocation event may be either a timeout or the execution of a construct that corresponds to accessing an object with a state-based mutual exclusion protocol (in Ada terms, a protected entry call). Intertask communication is through shared objects, either under software or hardware mutual exclusion control. Through the Ravenscar profile, Ada is unique in allowing the construction of portable, predictable, certifiable, concurrent programs.

Ada 2005 offers a number of improvements to the Ada language. Among the key enhancements are in the areas of object-oriented programming (OOP) interfaces, program packaging and an extensive containers library. See the sidebar “Ada 2005 Improves on Ada’s Strengths” on p.42 in this article.

Playing Nice with the Competition

Although Ada, and in particular Ada 2005, has substantial advantages over com-

```

1  pragma Profile (Ravenscar);
2
3  package Reader_Writer is
4    task Writer;
5    task Reader;
6  end Reader_Writer;
7
8  with Ada.Real_Time; use Ada.Real_Time;
9  package body Reader_Writer is
10
11    protected Position is
12      procedure Write(X, Y : in Integer);
13      entry Read(X, Y : out Integer);
14    private
15      X, Y : Integer := 0;
16      Readable : Boolean := False;
17    end Position;
18
19    protected body Position is
20      procedure Write(X, Y : in Integer) is
21        begin
22          Position.X := X;
23          Position.Y := Y;
24          Readable := True; -- Enables data to be read
25        end Write;
26
27      entry Read(X, Y : out Integer) when Readable is
28        begin
29          X := Position.X;
30          Y := Position.Y;
31          Readable := False; -- Ensures that data only read once
32        end Read;
33    end Position;
34
35    task body Writer is
36      X, Y : Integer;
37      Next_Time : Time           := Clock;
38      Period   : constant Time_Span := To_Time_Span (1.0); -- 1 sec
39    begin
40      loop
41        delay until Next_Time;
42        ... -- Obtain X and Y (e.g. from a hardware device)
43        Position.Write (X, Y);
44        Next_Time := Next_Time + Period;
45      end loop;
46    end Writer;
47
48    task body Reader is
49      X, Y : Integer;
50    begin
51      loop
52        Position.Read (X, Y);
53        ... -- Use X and Y in some computation
54      end loop;
55    end Reader;
56  end Reader_Writer;

```

(a)

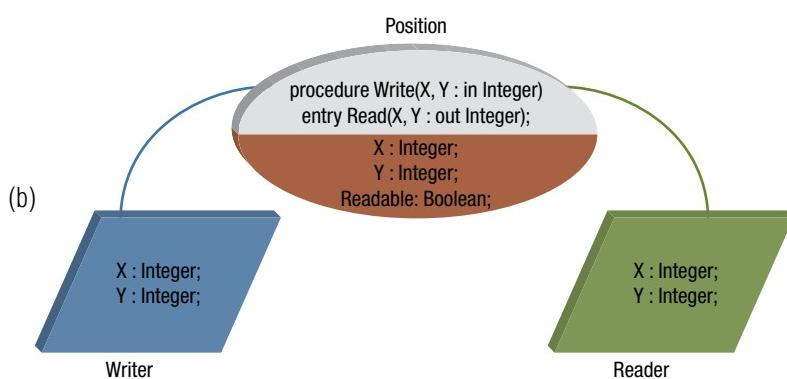


Figure 2

A program conforming to the Ravenscar Profile (a) comprises a fixed number of tasks where each task body is an infinite loop with a single “invocation event” at each iteration. The invocation event may be either a timeout or the execution of a construct that corresponds to accessing an object with a state-based mutual exclusion protocol—in Ada terms, a protected entry call. Intertask communication is through shared objects, either under software or hardware mutual exclusion control (b).

peting languages such as C++, Fortran and Java, in practice most large applications involve a mixture of languages. This makes good sense. Few large applications are actually programmed from scratch. Instead, developers try to make maximum use of existing reusable components, which may be written in a variety of languages. It makes no sense to rewrite these verified components in some other language. One of the less useful results of

the misinterpretation of the DoD's 1980s directives requiring Ada usage, was to encourage such rewriting (into Ada), when it made little sense, just as it makes no sense today to rewrite verified reliable Ada components in some other language.

But mixing languages can be problematic because most languages are designed with the conceptual notion that the entire program is in that language. Ada uniquely takes a more realistic view,

and specifically provides for interfacing to other languages in a well-defined way. At the time of the Ada 95 design, this larger view included C, Fortran and COBOL but not C++, since C++ had not yet been standardized. Now C++ has caught up in this respect, and Ada 2005 allows easy interfacing to C++ and also to Java (even though Java is not itself a standard).

Interestingly, in some respects a program comprising a mixture of Ada and C can be more reliable than one written just in C. For example, in some environments a callback to a user-supplied function requires that the function be compiled with a special calling convention. Failure to specify the needed calling convention, in a program written in C, can lead to a run-time crash. If the function is supplied in Ada and then passed to a foreign routine in C, the Ada compiler will detect the mismatch in calling convention and reject the program at compile time. This is much preferable to tracking down a run-time failure.

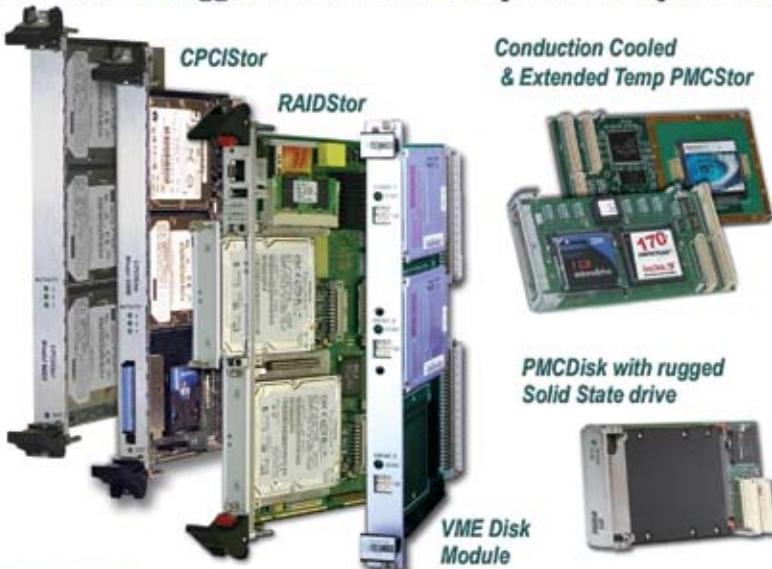
Ada 2005 Is Available Today

As noted earlier, Ada 2005 is not yet formally standardized. The ISO procedures, like those of any official organization, can take some time to complete. However, the important part of these procedures, namely the technical design, is complete today, and it is generally agreed that the final standard will be essentially identical to the proposal that exists today.

This means that there is no need to wait for formal approval to steam ahead. For example, AdaCore has made a major commitment to Ada 2005, and its products today incorporate the most important features of the proposed language. Complete implementations are expected during the first quarter of 2006. Combined with AdaCore's High Integrity Edition (HIE) version of Ada, which provides for flexible tailoring of subset capabilities, along with corresponding certification materials, this means that Ada 2005 is here today for use in the next generation of highly reliable software. ■

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Jeff Child

If the dynamics in the flash memory chip market and the roadmaps of flash chip vendors are any guide, it looks like flash-based solid-state disks (F-SSDs) are poised to quell any arguments for staying with traditional rugged hard drives. Throw in the major advantages in ruggedness and security that F-SSDs enjoy, and the contrast becomes even more vivid.

With no moving parts, F-SSDs are able to operate under the harshest conditions, unlike magnetic hard disk drives. In a rugged environment, the rotating mechanisms of a hard drive can fail, and are subject to partial and sometimes even total loss of data. Severe conditions including high shock, vibration, altitude, humidity and extreme temperature ranges increase failure rate percentages of hard disk drives, which is unacceptable for mission-critical systems.

Because F-SSDs targeted for military and aerospace apps use the same fundamental flash components as the consumer realm, the price advantages can be leveraged across all markets. The list of applications where F-SSD are attractive continues to broaden, now including submarines, space vehicles, aircraft carriers, high-altitude balloons,

high-speed locomotives, oil and gas pipelines, drilling rigs, weapons systems, mining equipment, combat aircraft and more.

Flash Tradeoffs Fade

Traditional drawbacks of flash-based disks are quickly falling by the wayside. Random access speeds rival and will soon beat other media, retention and re-writing cycles have dramatically increased and many systems offer a single-control erase-all function with or without power for security-sensitivity applications. All those factors have moved F-SSDs closer to the forefront as the lead option for rugged mass storage. Responding to the growing demand for F-SSDs, the major vendors of F-SSD products—including Adtron, BiTMICRO, M-Systems and Memtech—continue to ramp the capacity, performance and security features of their products.

Exemplifying the rugged environment capabilities of today's F-SSDs, BiTMICRO's solid-state E-Disk flash drive served as the data storage device for the Cosmic Rays Energetics And Mass (CREAM) project. The CREAM project is a NASA-sponsored high-altitude balloon experiment led by the University of Maryland in collaboration with other universities. The objective of this latest CREAM project was to investigate the composition of ultra-high-energy cosmic rays utilizing the Long Duration Balloon (LDB) vehicle technology developed by NASA.

The pilot-less, helium-filled scientific balloon and its CREAM payload were launched from the National Science Foundation's McMurdo Station, Antarctica on December 16, 2004. It traveled 41 days and 22 hours, breaking the previous unmanned balloon flight record of 31 days and 20 hours. All throughout the flight, CREAM instruments recorded about 36 Gytes of heavy nuclei data onto a 43 Gbyte E-Disk flash disk drive. Figure 1 shows the CREAM probe and its flight path.

Recently BiTMICRO Networks rolled out a military-grade version of its E-Disk 3S320, a Ultra320 SCSI F-SSD. Designed for extreme environments, the E-Disk Ultra320 SCSI can operate from -60° to +95°C and is designed to handle operating shock of up to 1500gs, making it an ideal storage solution for scientific missions and reconnaissance flights where data recording opportunities are critical.

The pure solid-state/non-volatile drive is OS-independent and is targeted to provide up to a 42 microsecond access time, 12,500 IOPS (max) and 2 million hours MTBF. Sustained read/write rate is 44 Mbytes/s (max) and burst read/write rate is 320 Mbytes/s (max). Available in a 3.5-inch form-factor, maximum capacity for the E-Disk Ultra320 SCSI is pegged at 155 Gbytes. The completely bootable drive comes with either a half pitch DB68 or SCA-2 ANSI-compliant connector and does not require any device driver for proper operation.



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Also climbing up the density curve, Targa Systems Division of L-3 Communications has boosted the available capacity for its Series 4 Removable Disk Data Transfer Systems to 36 Gbytes. The Series 4 DTU product line incorporates a 2.5-inch removable disk and is available in a compact ($k=4$) Dzus rail panel mount (CDU style) form-factor unit with either 28 VDC or 5 VDC power input. It is available with a multitude of interfaces, including USB and Ethernet. A hard mount version is also offered.

Serial ATA Solutions Roll

Serial ATA technology is quickly becoming the dominant interface for data storage devices migrating from the parallel ATA interface. Adtron's latest F-SSD offering is its 3.5-inch Serial ATA flash disk offering called the A35FB (Figure 2). The unit is built on Adtron's SmartStorage framework and the Adtron ArrayPr performance engine, and has a storage capacity of up to 128 Gbytes. Adtron's EraSure technologies further enhance the use of solid-state-based solutions in defense applications by providing clear and sanitize functions that are compliant with defense specifications.

Those features ensure rapid and secure data elimination from the media when required. Optional destroy, write protection and password protection features are also available. Both the A35FB flash disk and I35FB flash disk (its IDE counterpart) support either commercial (0 to 70°C) or industrial (-40° to 85°C) temperatures.

Likewise weighing in with a Serial ATA F-SSD offering, Memtech this summer announced the addition of SA2580, AT2580 and SA3580 Panther series of solid-state flash drives to its product portfolio. Performance ranges from 20 to 60 Mbytes/s, and capacities from 4 to 128 Gbytes. The Panther AT2580 is fully ATA-compliant and the Panther SA2580 and SA3580 are the next generation in SATA solid-state flash drive solutions.

The Memtech Panther series offers advanced security features, including se-

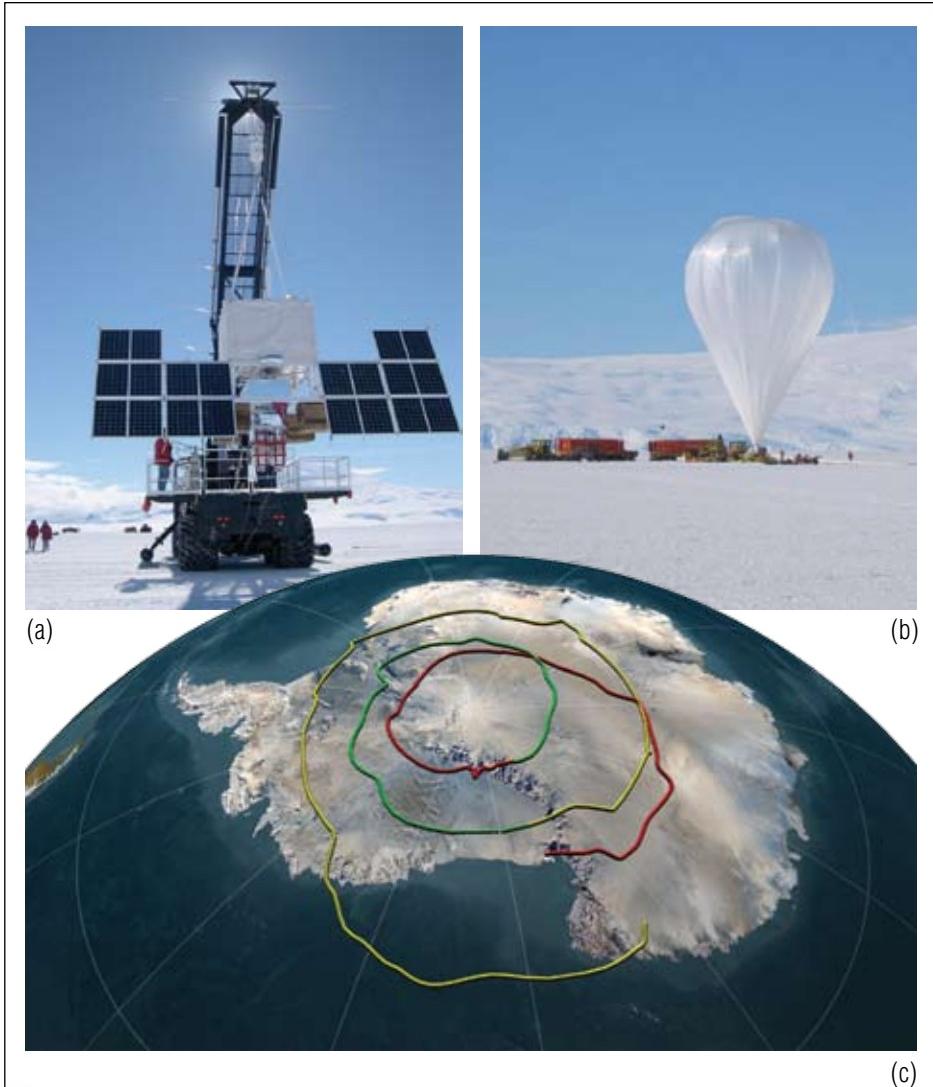


Figure 1

BiTMICRO's solid-state E-Disk flash drive served as the data storage device for the NASA-sponsored Cosmic Rays Energetics And Mass (CREAM) project. The CREAM project is a high-altitude balloon investigating the composition of ultra-high-energy cosmic rays utilizing the Long Duration Balloon (LDB) vehicle technology developed by NASA. The pilot-less, helium-filled scientific balloon traveled 41 days and 22 hours, breaking the previous unmanned balloon flight record of 31 days and 20 hours. The globe map image shows the balloon's path circling the South Pole three times. All throughout the flight, CREAM instruments recorded about 36 Gbytes of heavy nuclei data onto a 43 Gbyte E-Disk flash disk drive.

cure erase. The drives are designed for low power consumption in critical operating conditions and are built to withstand extreme temperature, pressure, moisture, shock, vibration and power loss. Each drive

is guaranteed for life and goes through a rigorous five-step temperature and ruggedness test process that includes read-write data integrity testing at temperatures as low as -40°C and as high as +85°C.

Special Feature



Figure 2

Exemplifying the trend toward Serial ATA F-SSDs, Adtron's latest F-SSD offering, A35FB, is a 3.5-inch Serial ATA flash disk with up to 128 Gbytes of storage capacity. Adtron's EraSure technologies further enhance the use of solid-state-based solutions in defense applications by providing clear and sanitize functions that are compliant with defense specifications. Those features ensure rapid and secure data elimination from the media when required.

M-Systems, meanwhile, is pushing the density curve for F-SSDs with their introduction of its FFD 2.5-inch serial ATA solid-state flash drive with up to 128 Gbytes of storage. The device features an endurance of more than 5 million write/erase cycles and an interface speed of 1.5 Gbits/s with a sustained read/write performance rate of 44 Mbytes per second. M-Systems' FFD SATA product complies with the stringent reliability requirements offset for mission-critical applications such as NEBS level 3 for the telecommunication industry and the MIL-STD 810F standard for military and aerospace.

Supporting stringent security standards required by military and other mission-critical applications, M-Systems' FFD 2.5-inch SATA is equipped with a fast security erase feature and complies with the sanitizing standards of the U.S. DoD, National Security Agency (NSA), Navy, Air Force (FSSI) and IREC (IRIG). ■

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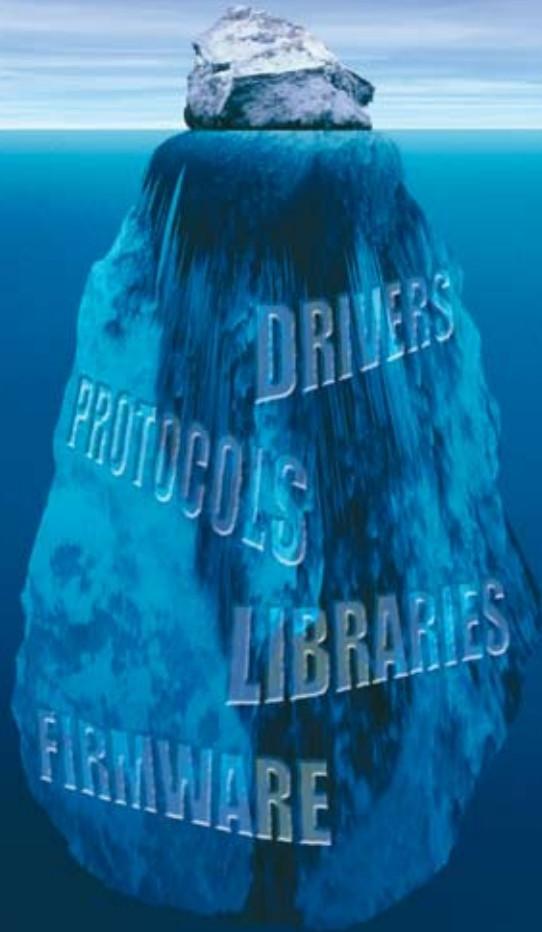
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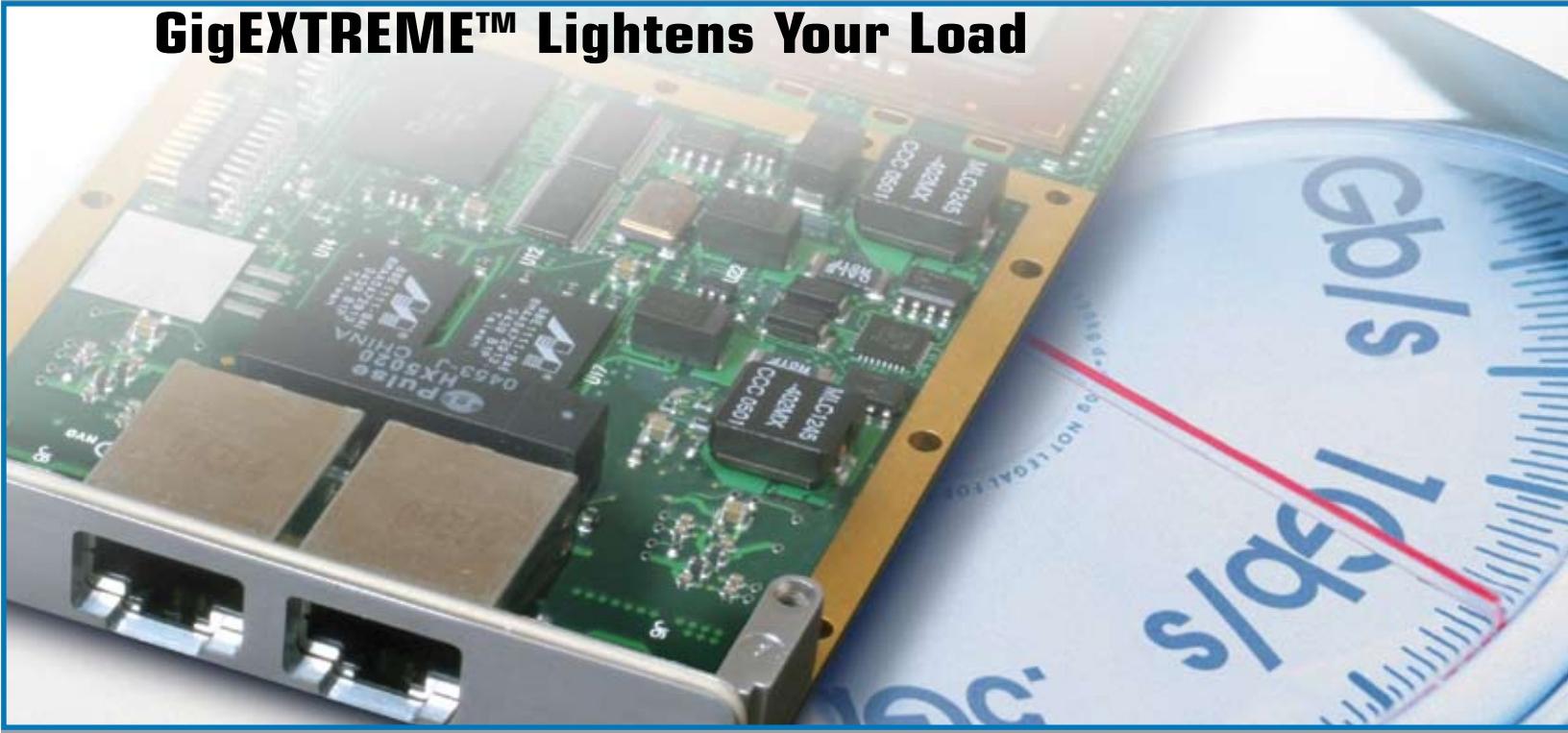


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* Processor loading measured for the TCP/IP receive network task on a 1 GHz Power PC host.



Special Feature

Mass Storage

Solid-State Flash Disks Migrate to Serial Interface Standards

When shock/vibration, altitude, humidity and temperatures are high, rotating hard disks become a real weak link. Flash disks offer a rugged, secure alternative.

Esther Spanjer, Technical Marketing Manager
M-Systems

With the ever-declining price of flash, storing the operating system (OS), application and data on reliable solid-state flash drives is becoming more viable as a data storage solution for design engineers. Like mechanical hard disk drives, solid-state flash drives are migrating from parallel to serial interfaces, such as Serial ATA (SATA) and Serial Attached SCSI (SAS), to provide higher read/write performances and reliability.

Hard disk drives (HDDs) are an inexpensive and high-capacity data storage media with an average failure rate of two percent, even in a controlled and air-conditioned environment. But take the HDD into a rugged mission-critical system and this rate can climb into the double digits. Mechanical failures in HDDs come in a variety of guises, such as read/write head

failures and motor problems. Conditions of high shock, vibration, altitude, humidity and extreme temperature ranges can potentially make the HDD the weakest link in mission-critical systems. Equally disturbing, HDDs leave traces of confidential data after erasure.

Solid-state flash disk drives are being designed as true "drop-in replacements" for mechanical HDDs in mission-critical applications. Unlike HDDs, flash disk drives are able to operate in the harshest environmental conditions defined in MIL-STD-810F: within -40° to +85°C temperature range, absorbing shock conditions at 1500g, and withstanding random vibration of 16g at 80,000 feet altitude. Flash disk drives can be erased without leaving any traces of data. Some also incorporate a power-free security erase feature in the absence of an external power source.

An example harsh environment application is the SaabTech Avionics' DiRECT Digital Recording System, an airborne digital recording system. The system integrates M-Systems' FFD 3.5-inch Ultra Wide SCSI flash disk as the storage media for three ongoing airborne



Figure 1

SaabTech won an order last year to produce its DiRECT Digital Recorder systems for the Spanish Air Force's F-18 Hornets. DiRECT integrated M-Systems' FFD 3.5-inch Ultra Wide SCSI flash disk as the storage media.



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Figure 2

Shown here are the most common flash disk form-factors: 2.5-inch (laptop size) and 3.5-inch (desktop size). With no moving parts, solid-state flash disk drives provide mean time between failure (MTBF) rates 10x higher than most HDDs, with an overall bit error rate (BER) of 10-20.

projects. DiRECT is a universal, digital mission recording system for use onboard aircraft. All critical information, such as video, audio and data recordings, is acquired and recorded by DiRECT. SaabTech won an order last year for series production of its DiRECT Digital Recorder and Data Transfer System, and associated ground-based systems, for the Spanish Air Force's F-18 Hornets (Figure 1). The new digital data recording system will replace the present tape recording system and is part of the upgrade program being carried out by EADS-CASA.

Costs Down, Capacities Up

Flash technology is becoming a commodity in consumer devices such as USB flash drives, flash cards for digital cameras and embedded flash drives in 3G mobile handsets. As a result of this huge demand, flash prices have declined dramatically over the past few years, a trend that industry experts expect to continue. The cost of flash is no longer an insurmountable barrier to using solid-state flash disks in mission-critical applications. In addition to cost decline, flash conforms to the industry's own version of Moore's law: every 12 to 18 months, double the capacity can be stored in the same silicon. This is packaged in a number of form factors to meet various industry requirements. Figure 2 shows the most common flash disk form-factors: 2.5-inch (laptop size) and 3.5 inch (desktop size).

Both mechanical HDDs and flash disk drives are migrating from parallel to serial interfaces. They support serial interfaces in data acquisition systems, such as serial ATA (SATA) and Serial Attached SCSI (SAS). They provide higher read/write performance and reliability, inherent in these new serial interfaces. In addition, new flash disk designs provide sustained read/write performance of more than 40 Mbytes/s and, due to the fact that flash does not require time to spin into action, the fastest OS boot time. Comparing average seek time, flash disk drives achieve performance in the range of 0.02-0.05 ms vs. HDD seek rates of between 3-7 ms. When comparing average latency, flash disk drives provide instant access vs. HDDs with an access time of 2-5 ms.

Parallel ATA	Serial ATA	SATA Advantages
Up to 133 Mbytes/s	Up to 150 Mbytes/s	Faster, and room for expansion
Tiny jumpers	No master/slave, point-to-point	Ease of use
Eighteen-inch cable	Up to 39-inch (1 m) cable	Ease of integration
Two-inch wide ribbon cable	Thin cable (1/4-inch)	Improved system airflow
80 conductor	7-wire differential (noise canceling)	Eliminates data integrity problems
40 pin and socket	Blade and beam connector (snap in)	Ease of use
Two-inch wide data connector	0.5-inch wide data connector	Ease of integration
On-board DMA controller	First-party DMA support	Performance enhancement
High 5V tolerance for legacy drives	Low voltage (0.25V) tolerance	Design improvement
Limited (legacy command queuing)	Intelligent Data Handling	Performance enhancement
—	Hot Swap	Ease of integration and use
CRC on data only	CRC on data, command, status	Enhanced data protection

Source: Seagate Technologies

Table 1

Compared here are attributes of parallel ATA and serial ATA, along with a description of SATA's advantages over parallel ATA.



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Parallel ATA vs. Serial ATA

Parallel ATA is the primary internal storage protocol to connect host systems to storage peripherals such as hard drives, flash disk drives, optical drives and removable magnetic media devices. The latest revision of the Parallel ATA is ATA/ATAPI-7, providing data transfer rates up to 133 Mbytes/s. The limiting factor on this rate is the physical characteristics of the parallel interface. Due to cross talk on the parallel lines, higher data transfer speeds would result in reduced reliability and unacceptable errors. Furthermore, the parallel ATA protocol was never designed to support hot swapping. These are the two main reasons why the next standard was defined as serial.

Serial ATA is the next-generation internal storage protocol, designed to replace parallel ATA technology. The Serial ATA-1 standard supports up to 150 Mbytes/s, with a roadmap already planned for 300 Mbytes/s and as high as 600 Mbytes/s for the next stage.

Table 1 shows a comparison between Parallel and Serial ATA. The key benefits of Serial ATA are: increased reliability due to the elimination of cross talk, hot-swap support and point-to-point usage. Especially for engineers struggling with BIOS settings and configuring master/slave and primary/secondary, this last advantage is a welcome change. A common misconception is that drives that support SATA-II must support 300 Mbytes/s. The name SATA-II was the name of the organization formed to author the SATA specifications. The group has since changed names to the Serial ATA International Organization, or SATA-IO.

Serial Attached SCSI (SAS)

The SCSI Trade Association followed suit with moving to a serial interface with the introduction of the Serial Attached SCSI standard. This new standard was designed to meet the ever-demanding needs of enterprise storage for high performance, high reliability and high manageability.

However, so as not to reinvent the wheel, they reached an agreement with the Serial ATA II workgroup in January 2003 to use the physical and electrical

	Serial ATA	Serial Attached SCSI
Performance	Half-duplex	Full-duplex
	1.5 Gbit/s (released) 3.0 Gbit/s (draft)	3 Gbit/s (draft) 6 Gbit/s (planned)
Connectivity	1m internal cable	> 6m internal cable
	One device	> 128 devices
Availability	SATA only	SAS and SATA
	Single-port drive Single host Point to point	Dual-port drive Multi-initiator Point to point
Software Transparency	ATA commands	SCSI commands

Table 2

This table compares the capabilities of Serial ATA versus that of Serial Attached SCSI.

interface of the SATA protocol in the Serial Attached SCSI (SAS) standard. This means that both Serial ATA and Serial Attached SCSI use the same physical and electrical interface. As a result, SATA drives can be physically connected to SAS hosts. The three software protocols that can run on top of this interface are:

- Serial SCSI Protocol (SSP)—supports SAS drives
- SATA Tunneling Protocol (STP)—supports SATA drives
- Serial Management Protocol (SMP)—supports SAS expanders

The SAS standard currently supports up to 3 Gbit/s data transfer speeds, with future rates planned for 6 Gbits/s and even 12 Gbits/s at the end of this decade.

Key end-user benefits of the standard include enterprise class robustness, investment protection in compatible SCSI software and middleware, and the choice of direct-attach storage devices (SAS or SATA). In addition, longer cabling distances, smaller form-factors and greater ease of device addressing will all lead to a new level of flexibility. Since SAS is based on the foundation of the industry-leading SCSI specification, it will satisfy users' needs for continuity in the mission-critical application.

SATA vs. SAS

Table 2 compares the characteristics of Serial ATA and Serial Attached SCSI.

SAS complements SATA by adding dual porting, full duplex, device addressing, and it offers higher reliability, performance and data availability services, as well as logical SCSI compatibility. Where SATA is targeted to cost-sensitive non-mission-critical desktop storage environments, SAS is clearly beneficial in demanding enterprise environments. Most importantly, these are complementary technologies based on a universal interconnect, where SAS customers can choose to deploy cost-effective SATA drives in a SAS storage environment.

Securing Confidential Data

Securing confidential data in emergency situations is essential for mission-critical systems. Security agencies in the U.S. define several levels of "erasing" sensitive data for various storage media type, such as tapes, magnetic disks and optical disks. Each U.S. military force has compiled its own internal version, drawn from the DoD/NSA instructions.

Since erasing is a generic term, several others terms are used:

Clearing: Clearing is the process of eradicating data on the media before it is reused in an environment that provides an acceptable level of protection for the data previously stored on the media before clearing.

Sanitizing (also called Purging): Sanitizing is the process of removing data on the media before it is reused in an envi-

ronment that does not provide an acceptable level of protection for the data previously on the media before sanitizing.

Destroying: Destroying is the process of physically damaging the media to make it totally unusable as a media, thereby making it impossible to retrieve data.

Sanitizing mechanical disks and magnetic tapes is an arduous process, requiring

special degaussers, stable power conditions during the process and ample time, all of which may be lacking during an emergency. Solid-state flash disk drives are available that can sanitize the disk in seconds with fast secure erase and sanitize procedures. Once fast secure erase has been activated, auto-resume secure erase guarantees successful completion of the process.

M-Systems released the first Serial ATA flash disk drive to the market in June 2005, with other solid-state disk vendors following suit thereafter. M-Systems' offering includes a 2.5" Serial ATA drive, with capacities up to 128 Gbytes (to be doubled in mid 2006), burst performance of 150 Mbytes/s and sustained read/write speeds of 44/40 Mbytes/s. The drive can be partially or completely erased/sanitized via a software or hardware interrupt, in full compliance with all common military specifications. With the fast security erase feature, a 128 Gbyte drive can be erased in a bit over 9 seconds.

Rapid Adoption Rate

Due to demands in increased reliability and performance, the embedded industry is adapting serial interfaces at a rapid rate. In 2006, hard disk drives that support SATA or SAS interfaces will be an estimated 40% of all hard disk shipments. According to market research firm IDC, this is expected to grow to more than 70% by 2008. Solid-state drives will follow this trend, and with flash prices declining at a rate of 30-40% yearly, they are becoming an attractive alternative to failure-prone mechanical hard disk drives in many applications. When securing and erasing confidential data is key, solid-state disk drives provide a far easier and faster solution. With a simple software or hardware command, it is possible to erase large-capacity solid-state drives in a matter of seconds. ■■

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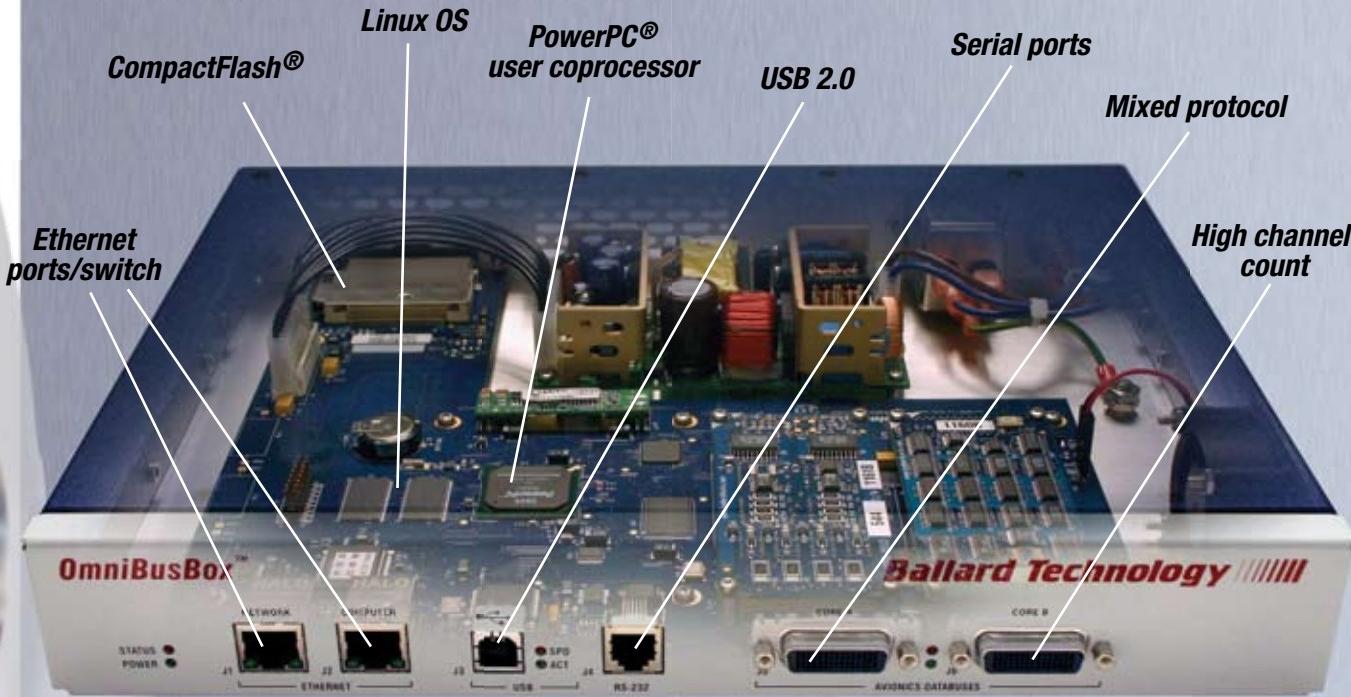
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Analyzer Tools Tame PCI Express Complexities

PCI Express has entrenched itself into many board form-factors suited for military use.

PCI Express protocol analyzers help smooth development chores.

Jeff Child

PCI Express certainly wasn't the first switched fabric technology on the block, but as it moves onto servers and desktop PCs, it's already becoming the most ubiquitous. And it's rapidly moving into the embedded-computer space. And like all the other switched fabrics, PCI Express came into existence long before the military market expressed any interest in switched fabrics.

From expansion in VME and cPCI standards organizations, which have already incorporated PCIe into their next-generation specs, to a variety of other standard and stand-alone SBC products, PCI Express is rapidly becoming a backbone of performance-based embedded systems. Table 1 shows a cross section of some of the embedded board-level form-factors that incorporate PCI Express.

As military system developers step up their efforts to implement PCI Express technology into their designs, they must understand just how radically different PCI Express is from traditional parallel buses. Those differences are reflected in the current sophisticated crop of PCI Express Analyzer tools that have emerged.

With traditional parallel buses—like PCI, PCI-X and VME—all of the protocol signals associated with data transfer are simultaneously presented and act in parallel. Developers can see bus signals and interpret bus conditions by simply capturing and viewing the raw signals with relatively simple development tools. Serial bus topology, however, is vastly different and presents new challenges in the test and debug phases of device development. These challenges extend beyond the abilities of simplistic measurement instruments, and require more advanced tools and test processes to implement PCI Express buses.

Serial bus protocols also require additional headers and footers, such as CRC, to ensure data transfers are secure and error-free. These additional bits are included in the data packets and require additional interpretation, further increasing the complexity of validation and the test process.

Communication Across Multiple Layers

Adding yet another twist, the PCI Express architecture has defined protocols that communicate in several different layers. The "Physical Layer" protocol is used for establishing and maintaining the links; the "Data Link Layer Packets" protocol is used for hand

shaking; and the "Transfer Layer" protocol is used for transferring the data. To interpret PCI Express bus conditions adequately, developers must be able to convert raw bits into the specific layers.

Unlike the parallel-based PCI architecture, where the start and end of a transfer can be seen on the same bus, PCI Express is a dual simplex architecture. This architecture requires the requester to transmit a "Request" for data transfer on one transmit pair, while it receives the "Completion" response on the receive signal pair, which is a different bus. Considering the response time can vary widely, developers need the ability to filter the received and transmitted data independently of each other.

These unique attributes lead to a more complex process for monitoring and interpreting PCI Express buses. In addition, converting binary bits into a meaningful interpretation of the various protocol layers of PCI Express requires advanced and dedicated tools that extend beyond the capability of general-purpose measurement instruments.

Fortunately, a mature set of PCI Express analyzer tools is available to help developers navigate the intricacies of the PCI Express specification. The product roundup on the next two pages details the capabilities and features of a sampling of PCI Express analyzer offerings. ■

Form-Factor	PCI Express Lanes	Size (inches)
AMC Express (AMC 1.2)	x4	2.9 x 7.1, 5.8 x 7.1
ATCA Express (PICMG 3.4)	x4	12.7x11
COM Express	x1	3.7x4.9, 4.3x6.1
Compact PCI 3U Express	x1, x4, x8, x16	3.9x6.3
Compact PCI 6U Express	x1, x4, x8, x16	9.2x6.3
CompactTCA 6U Express	x5	9.2x6.3
EPIC Express	x1, x4	6.5x4.5
VITA 41	x8	9.2x6.3
VITA 46	x8	9.2x6.3
XMC Express (VITA 42)	x4	2.9 x 5.9, 5.9 x 5.9

Table 1

The PCI Express switched fabric has already found its way into numerous standard embedded board form-factors.

Technology Focus: PCI Express Analyzers Roundup

System Support Multiprotocol Bus Analysis

Complex military systems often rely on numerous data bus and I/O interconnect technologies. An ability to analyze several such interfaces simultaneously helps simplifying test chores. Along such lines, Agilent's E2960A, a set of test tools for analyzing and exercising PCI Express bus protocols, provides multiport testing capability that lets users stress all slots with the same load conditions and synchronize the tests.



The platform provides a full-speed x8, x4 and x1 combined exerciser-analyzer unit for PCI Express. External trigger in/out enables synchronization with other devices. A device can be connected with a non-intrusive passive or active slot/interposer probe or a soft touch midbus probe. The system, combined with other Agilent products, lets you do multiprotocol test/cross bus analysis and simultaneously record PCI Express, Fibre Channel and Advanced Switching Interconnect traffic and transactions and time-correlate them within the same test setup and graphical user interface (GUI).

The system's GUI offers a flexible approach to control the exerciser either through an API such as Command Application Interface (CAPI) or Tool Command Language interface, or through the GUI. This option allows very quick test setups with the GUI, or more comprehensive test coverage with the API.

The protocol analyzer, including Agilent's patented dynamic trigger conditions, is the core debug and bring-up test tool for root cause analysis, troubleshooting and performance analysis. It provides non-intrusive monitoring of PCI Express traffic between either an add-in card and a system or between a protocol exerciser and a system. Pricing for the Agilent E2960A analyzer ranges from \$15,999 to \$39,990 depending on configuration.

Agilent Technologies
Palo Alto, CA.
(408) 654-8675.
[www.agilent.com].

PCIe Root Complex Testing Added to Analyzer Suite

Ensuring full compliance to the PCI Express specification is a complex process. The more test suites brought to bear on the task the better. Catalyst Enterprises recently made a major expansion to its SpekChek PCI Express compliance test package. This new addition provides a comprehensive, automated test suite for PCI Express root complex devices and complements the existing SpekChek test suite for endpoint devices. With this new addition to SpekChek, Catalyst now has nearly 600 individual test cases for confirming endpoint and root complex compliance to the PCI Express specification.

Each test case in SpekChek's endpoint suite is derived directly from compliance requirements documents provided by the PCI Special Interest Group (SIG). As tests are executed, capture files are maintained for review and debug purposes. A comprehensive pass/fail



report is automatically generated at the end of the automated testing process. SpekChek is a software add-on to Catalyst's SPX Series of PCI Express analyzers and exercisers. Existing SpekChek customers may upgrade to the root complex test suite at no cost.

The Catalyst SPX Series of PCI Express products is provided to support lane configurations from x1 to x16. For x4 and below, Catalyst provides a single-board PCI Express analyzer/exerciser system, providing both passive in-line protocol analysis capabilities between two link devices, active endpoint or root complex emulation, protocol error detection, error injection and automated compliance testing. For designs at x8 through x16, the SPX Series offers two separate boards, one optimized for analysis and another optimized for exercising functions.

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(408) 365-3846.
[www.getcatalyst.com].

Analysis Probe Features Drill-Down GUI

One of the roles of an effective bus/protocol analyzer is its ability to display transaction data in a way that facilitates problem solving. FuturePlus Systems does just that with its FS4400 product, a PCI Express protocol analysis probe for use with Agilent Technologies' logic



analyzers. The FS4400 marks the introduction of the new Transaction Viewer software, which presents bus transactions in a graphical, horizontal-bar view that allows users to drill down to see transaction details. The analysis probe also includes software that decodes and displays bus data as protocol, hex or binary data. Configuration files are also provided to facilitate rapid logic-analyzer setup.

The FS4400 allows non-intrusive probing of PCI Express buses at a data rate of 2.5 Gbits/s. Several different optional probe adapter cables offer mid-bus probing or interposer probing of x1, x2 and x4 links, including ExpressCard. The FS4400 will handle one or two unidirectional links, or one bi-directional link.

Other FS4400 features include simultaneous monitoring in two directions on x1, x2 and x4 links along with 2- and 4-lane de-skew in both 8b and 10b data modes. The unit detects packet types and checks packet delimiters. Also included is user-enabled descrambling and packet-aware data filtering and logic analyzer triggering. User-selectable lane reversal and polarity inversion is provided as well as a USB port for probe control from a PC. While many newer bus analysis probes are designed to work only with the newest generation of logic analysis modules, the FS4400 is compatible with most Agilent16700- and 16900-series modules. The FS4400 has a list price of \$15,000, less probe adapter cables.

FuturePlus Systems
Colorado Springs, CO.
(719) 278-3540.
[www.futureplus.com].

Logic Analyzer Boasts PCIe Support Package

It's rare that system designers have only one bus protocol that they need to analyze. With that in mind, an alternative to a stand-alone PCI Express analyzer is a full-featured logic analyzer system that offers a PCI Express support option. An example is Tektronix's TMS817/818 support package that provides an interface between a PCI Express link and the TLA700 Series logic analyzer. Logic analyzers, used in conjunction with the TMS817, provide real-time trace visibility across all lanes of up to a x16 link and can automatically time-correlate signal activity across multiple computer or communications systems.

A TLA700 logic analyzer with a TMS817 preprocessor provides designers complete PCI Express real-time electrical and packet visibility. It acquires signals at full PCI Express speeds of 2.5 Gbit/s. The unit provides clock recovery as well as deskewing, decoding and descrambling of data. Triggering can be done on packet attributes and cross-triggering other instruments. The system lets you filter out unwanted data in real time and let you filter and search for data after the acquisition. Time-correlating of data is enabled across multiple buses. And data is displayed in user-selectable formats.

The TMS817 provides two methods to connect to the bus. The recommended method to access a PCI Express bus is to include one of two specific landing pads, called the midbus



footprints, on the PCI Express bus trace. The TMSIC6 interfaces to a midbus footprint with 16 differential pairs. This footprint is ideally suited to probe a full duplex x8 link or ½ of a x16 link. The second method to connect uses slot-style interposers to adapt two midbus probes to x16, x8, x4 or x1 PCI Express-compliant connectors.

Tektronix
Beaverton, OR.
(800) 835-9433.
[www.tek.com].

Analyzer Supports XMC Form-Factor

XMC, the PCI Express Mezzanine Card defined in the VITA 42.3 specification, is destined to become one of the most common paths for PCI Express to play in the board-level embedded space. Supporting that trend, VMETRO expanded its Vanguard analyzer family with the introduction of the Vanguard Express PCI Express Protocol Analyzer. Designed for debugging, testing and validating the PCI Express protocol, the Vanguard Express analyzer allows testing of x1, x4 and x8 PCI Express card-edge and XMC form-factors.



According to VMETRO, the Vanguard Express is the only PCI Express analyzer offered for the XMC form-factor.

The Vanguard Express is designed to offer maximum flexibility for multiple form-factors. In an XMC environment, a device under test is installed on top of the Vanguard Express analyzer. In the PCI Express card-edge form-factor, the Vanguard Express installs between the system slot and the device under test.

The Vanguard Express is operated via USB or Ethernet while using VMETRO's BusView 5 Graphical User Interface software running under Windows 2000 and XP. A single workstation can control multiple Vanguard analyzers for monitoring different protocols, like PCI-X/PCI, PMC, CompactPCI or VME. The Vanguard Express supports advanced decoding of the PCI Express protocol. This decoding includes viewing the trace data in lane, packet and data views, thus making the captured data easy to read and interpret for all users, regardless of expertise and task. Other features include x1, x4 and x8 link support, 256 Mbyte trace buffer, eight trigger events, independent and concurrent operation of the analyzer and the statistics and protocol checker.

VMETRO
Houston, TX.
(281) 584-0728.
[www.vmetro.com].



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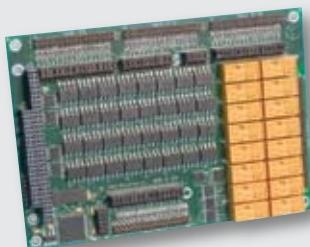


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EPIC Expansion Card Targets PC/104 High-Voltage Apps

Many high-performance, high-voltage defense applications require high-voltage relay switching as well as excellent signal isolation. To fill that need, the EPIC-footprint EPIC182 expansion card from Micro/sys targets PC/104 high-voltage applications by offering 64 lines of opto-isolated digital inputs and an additional 16 relays for isolated I/O signaling.

Each of the EPIC182's 64 isolated inputs can handle 3 VDC to 50 VDC while providing 4 kVrms isolation between the input signal and the system. A user-selectable, pull-up/pull-down resistor allows each input to be individually pulled high or low to ensure a known logic level at power-up. Sixteen lines of 1.5 kVAC isolation are available using 16 Form-C relays that also offer 250 VDC isolation between relays. The Form-C relays provide a switching capacity of 2 Amps at 30V. For improved system reliability, the relays' current states can be read. The relays retain their states during board power-up or power-down.

The EPC182 operates from a single 5V supply and draws 1.5A (max) 330 mA (typ - no relays energized). It has a flexible I/O base address range and 16-bit pass-through connector. Operating temperature range is -40° to +85°C. Price is \$375 in single quantities.

Micro/sys, Montrose, CA. (818) 244-4600. [www.embeddedsys.com].



Rugged, Single-Slot SBC Provides 2eSST VMEbus Performance

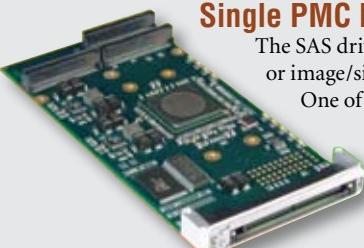
The SBCs used in high-performance, intensive military and aerospace applications require very high levels of performance and a lot of ruggedness. One way

of achieving this is by utilizing the 2eSST protocol, which runs native on VME. The C6100 ruggedized, single-slot SBC from Aitech Defense Systems implements the 2eSST protocol by incorporating Motorola's Tundra Ts1148 VMEbus interface chip to provide 320 Mbytes/s in most applications.

The C6100's low-power MPCC7457 G4 PowerPC processor operates at 1.276 GHz and incorporates DSP-like AltiVec technology, making the board suitable for a variety of vector processing applications. In addition, the board's standard design enables its installation into any IEEE 1101.2 conduction-cooled VME chassis or ANSI/VITA 1-1994 standard air-cooled chassis.

The C6100 supports legacy MVME761 and MVME712M I/O modules and provides up to 2 Gbytes of DDR ECC-protected SDRAM and 128 Mbytes of onboard programmable user flash. Two PMC slots are provided for I/O expansion, along with two Gigabit Ethernet interfaces and two asynchronous serial ports. VxWorks and Linux RTOS are supported. Both rugged and military operating temperature ranges are available. Pricing starts at \$6,750.

Aitech Defense Systems, Chatsworth, CA. (888) 248-3248. [www.rugged.com].



Single PMC Board Is Quad Port SAS Disk Controller

The SAS drive controllers used in storage systems for military applications—such as distributed computing, video-on-demand or image/signal processing—deliver data transfer rates of up to 3 Gbits/s per interface while leveraging existing SCSI protocols.

One of the first quad port SAS disk controllers on a single PMC board is the SC PMC/SA1 from Concurrent Technologies.

The SC PMC/SA1 provides four independent SAS and/or SATA ports utilizing the LSI Logic LSISAS1064 serial drive controller. The board can support serial link connections for up to four SAS 1.0- or four SATA 1.0a-compatible HDD, or a combination of both interfaces. Each link operates at either 1.5 Gbits/s or 3 Gbits/s. All serial attached device protocols, such as SSP, SMP, STP and SATA, are supported, as well as 2-, 3- and 4-lane SAS wide port configurations.

The board's PMC PCI interface supports 32/64-bit 33/66 MHz PCI buses and 3.3V PCI signaling. Two Mbytes of flash EPROM are pre-programmed with the LSI PC BIOS and onboard configuration utility, and 32 Kbytes of NVRAM are provided for configuration data and nonvolatile RAID information. Linux, Windows 2000, Windows Server 2003 and Windows XP are supported. List price is \$790.

Concurrent Technologies, Ann Arbor, MI. (734) 971-6309. [www.gocct.com].

Dual-Core PICMG 1.3 Board Targets 32-Bit/64-Bit Computing

As 64-bit computing shifts into the mainstream, processors like AMD's Opteron are expected to entrench themselves as forces to be reckoned with. But 32-bit technology must also be accommodated. The full-size PICMG 1.3 MB-06049 system host board from WIN Enterprises is powered by AMD's Opteron processor and enables both 32-bit and 64-bit computing.

The MB-06049 PICMG 1.3 supports either a single- or dual-core CPU, and a full range of Opteron processors, from low to high power. A HyperTransport interconnect system enables quad-core designs by allowing the additional integration of one or two dual-core processors on stackable boards. The MB-06049 includes the NVIDIA nForce Professional 2200 chipset.

A 20-lane PCI Express slot is also featured. The board includes two memory slots totaling up to 8 Gbytes. Two additional memory slots with an optional CPU adapter card yield a total of 16 Gbytes. Interfaces include standard IDE, 4X SATA with RAID, 1 Gigabit Ethernet and four USB 2.0.

The MB-06049 supports Linux Debian 64 and Windows XP 32- and 64-bit operating systems. Evaluation products are available now with production volumes in January 2006. Without CPU or memory, prices are \$1,000 for the single-processor version and \$1,200 for the dual-processor version.

WIN Enterprises, N. Andover, MA. (978) 688-2000. [www.win-ent.com].



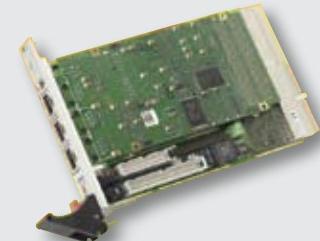
LED-Backlit TFT LCDs for High-Res Displays

An increasing number and variety of military systems must display data accurately on LCD displays. A new family of LCDs from Apollo Display Technologies is designed for the high-resolution display of color images from static to full-motion video.

The Optrex family of TFT LCDs, backlit by long-life white LEDs, is available in diagonal sizes of 6.5-in., 8.4-in., 10.4-in. and 12.1-in. The 6.5-in. LCD is available in VGA resolution, the 8.4-in. in VGA or XGA resolution, the 10.4-in. in VGA or SVGA resolution, and the 12.1-in. in SVGA or XGA resolution. The 6.5-in. VGA LCD provides a brightness of 390 cd/m², while sizes of 8.4-in. and up are backlit by ultra-high bright white LEDs and offer luminances ranging from 250 to 600 cd/m².

A range of performance enhancement options for the Optrex TFT LCDs include anti-reflective front surface treatment for daylight readability, an ultra clear touch sensor with 87% light transmission and a single- or dual-rail white LED constant current driver board with analog and PWM dimming capabilities. Other available options are brightness enhancement film, protective overlay, touchscreen, controller board, SBC kit and open frame monitor. Pricing starts at \$198 each for a 6.5" VGA LCD in production quantities of 10,000 units.

Apollo Display Technologies, Ronkonkoma, NY. (631) 580-4360. [www.apolloDisplays.com].



Rugged CompactPCI SBC with MPC5200 PPC Features FPGA

Embedded mobile defense applications, such as transportation systems, require lots of functionality in demanding environments. With those needs in mind, Men Micro has introduced the F12, a rugged, single-slot 3U CompactPCI SBC based on a 384 MHz MPC5200 PowerPC. The F12 includes an Altera Cyclone FPGA for graphics or other custom I/O.

The MPC5200 processor includes a telematics communications unit, floating-point unit, memory management unit, DRAM controller and the BestComm/DMA I/O controller, which can drive a number of interfaces such as CAN, USB, Fast Ethernet and SPI. Onboard storage resources include up to 256 Mbytes of SDRAM, 1 Gbyte of NAND flash memory, 2 Mbytes of static RAM and 16 Mbytes of graphics RAM. For expansion, two Fast Ethernet ports, a serial communication (COM) port and one USB interface are included. An optional version has robust D-Sub connectors in lieu of the standard RJ45 connectors. Two CAN channels are also available with the addition of Men Micro's small SA-Adaptor transition modules.

The F12's operating temperature range is -40° to 85°C. To help reduce the effects of shock and vibration, all onboard memory is soldered to the PCB. Comprehensive board support packages based on Men Micro's BIOS for PowerPC processors, MENMON, are available for Linux, VxWorks and QNX. Pricing starts at \$954 for single units.

Men Micro, Dallas, TX. (512) 267-8883. [www.menmicro.com].



Signal Processing Card Delivers 16x Improvement in D/A Resolution

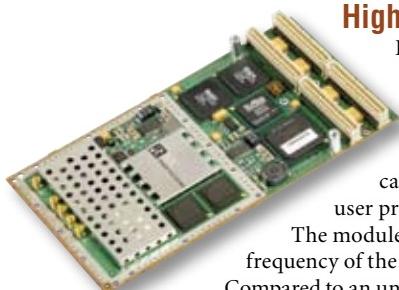
Demanding military signal processing applications such as radar, beamforming, electronic warfare and electronics countermeasures systems can be a challenge to design when they must operate in noisy environments. Performance can be improved dramatically when both A/D and D/A conversion are provided on a single card. The Triton VXS-1 from TEK Microsystems is the first 6U

VME/VXS payload card to include both, along with FPGA technology, for designing systems with higher recognition accuracies.

The Triton VXS-1 includes a 12-bit, 2.0 Gsamples/s D/A converter and a 10-bit 2.0 Gsample/s A/D converter, delivering a 16x improvement in currently available digital to analog resolution. In addition, the digital processing system is moved closer to the overall system's front end, eliminating RF components and increasing reliability.

Enhanced channel-to-channel synchronization between the VXS-1 and multiple Neptune 2 cards supports applications that require up to 32 channels to remain coherent to within one sample. Because of the precise synchronization between A/D and D/A conversion channels, low latency in active systems can be achieved between the sampled input and the corresponding output. Consequently, phase jitter on output signals is reduced, leading to higher-fidelity transmitted signals. Pricing starts at \$31,000 for single unit quantities.

TEK Microsystems, Chelmsford, MA. (978) 244-9200. [www.tekmicro.com].



High-Performance A/D Converter PMC Module Targets Harsh Environments

Designers of systems for software defined radio, military communications, signal intelligence and intercept in the field, radar and test and measurement applications need very high-performance A/D conversion. With that in mind, Interactive Circuits & Systems, Part of Radstone Embedded Computing, has introduced the ICS-8552 ADC PMC module.

The ICS-8552 is based on Texas Instruments' ADS5424 high-performance bipolar A/D converter, capable of sustained 105 MHz sample rates at temperatures of up to +85 °C. A 3,000,000-gate FPGA provides user programmability and enables processing to occur closer to the antenna, resulting in higher system throughput.

The module's high-stability, high-precision temperature-compensated crystal oscillator (TCXO) ensures that the frequency of the clock does not drift with changes in temperature.

Compared to an uncompensated clock, typically accurate to 20 parts per million (ppm), and higher quality clocks, typically accurate to 10 ppm, the ICS-8552 TCXO is accurate to only 1 ppm. This level of performance makes the ICS-8552 suitable for long acquisitions and FFTs, while its low noise (70 dB SNR, 80 dB SFDR) ensures maximum signal purity and integrity. Pricing starts at \$4,947 in OEM quantities.

Interactive Circuits & Systems, Part of Radstone Embedded Computing, Ottawa, Canada. (613) 749-9241. [www.ics-ltd.com].



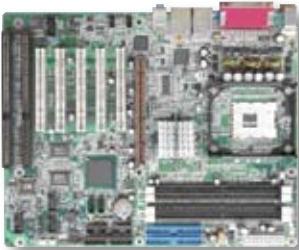
Universal Network Analysis Tool for Controller Area Networks

Designers of military systems that use CAN networks face the demands of growing system complexity. To help alleviate this situation, Accurate Technologies has developed CANLab, a universal network analysis tool for monitoring and logging messages and signals generated on a CAN.

Designed using .NET technology, CANLab provides the ability to send messages over any available network channel, facilitating the ability to re-send recorded bus traffic. Additionally, real-time data and data imported from previous recordings can be viewed simultaneously for in-depth post-analysis. Messages and signals transmitted from any available network channel can be displayed and manipulated in a variety of ways. The CANLab Workspace screens can be configured through a docking window management scheme.

The tool offers a full-featured scripting engine, letting users programmatically interact with the CANLab run-time environment. Complex functions can be composed to respond to several different types of events. CANLab supports Windows 2000 and XP, is compatible with C++ and requires a processor running at 500 MHz or faster with at least 128 Mbytes of RAM. It supports a wide variety of CAN interface hardware, including Kvaser v3.8 and Vector v4.3, as well as both .DBC and .UEF database formats. Prices start at \$2,000.

Accurate Technologies, Wixom, MI. (617) 739-8693. [www.accuratetechnologies.com].



Pentium 4 Motherboard Is Intel VRD 10.1-Compliant

The systems used in demanding, compute-intensive military applications must also be flexible enough to be easily upgraded with new processors. With that in mind, the ATX-865G P4 motherboard from Arista is Intel VRD 10.1-compliant to support future processors.

The ATX-807 CPU includes a 400/533/800 MHz FSB Pentium 4 Prescott (90 nm) CPU and four DDR DIMM sockets that support up to 4 Gbytes of DDR 266/333/400 unregistered non-ECC memory. The board features an 865G integrated Intel Extreme Graphic Engine with a 266 MHz core frequency and onboard 100/10 Intel 82547GI and 82541GI Ethernet controllers.

The ATX-865G board has eight USB 2.0 ports that support USB hot-plug. For expansion, there are one high-speed parallel port with SPP/EPP/ECP mode support, four 16550 UART-compatible ports, a pin-header connector for an optional IrDA external connector, two Enhanced PIDE interfaces and support for up to two SATA-150 HDDs. An FDD interface supports up to two floppy drives, and two ISA slots are provided for applications that use ISA legacy cards. Pricing starts at \$365.

Arista, Camarillo, CA. (510) 266-1800. [www.aristaipc.com].

Rugged PCI-X Platform Targets Portable Needs

Defense engineers often need a rugged, portable PC-based platform for a variety of uses, such as field testing. The new portable FlexPAC PCI-X E4 platform from Kontron America, based on passive backplane technology, is space-efficient and expandable.

Equipped with a Xeon E4 2.8 GHz processor, the FlexPAC PCI-X E4 provides a three-slot, full-size backplane, one PCI-X 133 MHz slot and two PCI-X 100 MHz slots. It features a dual Gigabit LAN controller, built-in Serial ATA controller and a Mini PCI slot. The system includes



from 512 Mbytes up to 4 Gbytes of RAM, 16 or 32 Gbytes of VRAM, an integrated 40-Gbyte EIDE HDD, CD-ROM and FDD with optional CD/DVD-writer, a 14-in. XGA TFT display, and an internal 100-250 VAC, 50/60 Hz AC power supply.

The FlexPAC rugged aluminum chassis-within-a-chassis construction and its card retention systems ensure that expansion cards are secured and protected. Operating temperature range is 0° to +50°C. Pricing for single quantities is \$6,375.

Kontron America, Poway, CA. (888) 294-4558. [www.kontron.com].



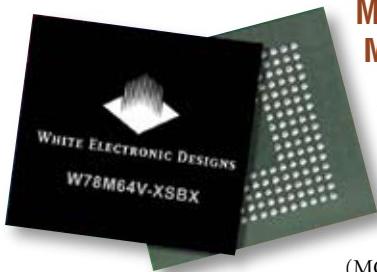
Ultra-Rugged Portable PXI Test Set Targets Field Testing Apps

Military engineers often need to perform PXI-based data acquisition and testing under harsh conditions. The Geotest MTS-207 is an ultra-rugged, portable PXI-based configurable platform for field testing and data acquisition systems.

Inside its rugged enclosure, a 14-slot PXI chassis mainframe has one slot dedicated to a 6U PXI controller. Slots two through seven can accommodate either 3U or 6U PXI/CompactPCI instruments. Slots eight through fourteen accommodate only 3U PXI/cPCI instruments. Available controllers for the MTS-207 include 1.2 GHz and 1.7 GHz Pentium 4 CPUs. The MTS-207 also provides sufficient space for custom circuitry, such as specialty power supplies and circuit cards. Fan assemblies provide dedicated cooling to the PXI chassis and internal circuitry. Multiple shock mounts and extensive internal temperature sensors ensure reliable operation under adverse operating conditions.

An optional Remote Control & Display Unit (RCDU) combines an LCD display with a touch panel for operation from a distance of up to 25 feet in environments where a keyboard and mouse are not functional or practical. Optional built-in heaters for the PXI chassis and the RCDU allow the MTS-207 to operate in extremely low temperatures. Prices begin at \$25,000.

Geotest, Irvine, CA. (949) 263-2222. [www.geotestinc.com].



Multi-Chip Package Device Serves Up 64 Mbytes of Flash

Densities of flash memory have reached a point where complete, complex embedded programs can reside in solid-state memory without the reliability risks of a magnetic disk for storage. Feeding the harsh environment, mil-temp segment of such demands, White Electronic Designs Corp. (WEDC) announced availability of its 64 Mbyte Flash multi-chip package (MCP). As the latest member of the WEDC family of Flash

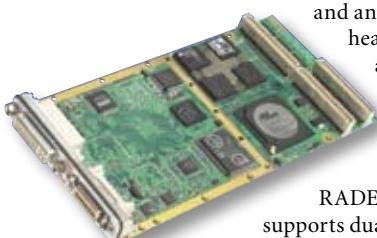
MCPs, this component is designed to complement high-performance processors and memory controllers for embedded and high-reliability applications and is available in commercial, industrial and military temperature ranges.

The 64 Mbyte Flash is in a 13 x 22 mm², 159 plastic ball grid array (PBGA) 286 mm². Organized as 8 Mbit x 64, the flash features access times of 90, 100 and 120 ns with 1 million erase/program cycles per sector. The component has zero latency between read and write operations and data can continuously be read from one bank while executing erase or program functions in another bank. The package offers 3.3V for read, erase and write operations. The device also offers both top and bottom boot block architectures. The 8 Mbit x 64 Flash PBGA, defined as part number W78M64V-XSBX, is priced at \$250 each in volumes of 500 pieces.

White Electronic Designs, Phoenix, AZ. (602) 437-1520. [www.wedc.com].

PMC Blends Video Capture, Dual-Channel Graphics

Saving board slots saves system integrators time and cost. Both are important, particularly in benign military environments where cost controls can be tight. Curtiss-Wright Controls Embedded Computing mixes several functions onto a single mezzanine, with its new video-capture enhanced member of its Atlas family of dual-channel, high-resolution PMC graphics controllers. The new



AtlasPMC/2 PMC card delivers video, RGB and DVI input capability and an extensive range of multimedia features including dual-head analog or DVI output display, stereo audio I/O and an onboard USB 2.0 controller. The AtlasPMC/2 saves slots and eases the integration of powerful, flexible multimedia functionality in VME, CompactPCI and PCI systems.

The AtlasPMC/2 is based on ATI Technologies' RADEON Mobility 9000 (M9) mobile graphics processor, which supports dual 2D, 3D, OpenGL and DirectX compatible displays with up to 16.7 million colors (24 bpp). In addition to its 64 Mbytes of integrated memory, the Windows-compatible M9 delivers advanced features such as reduced-power optimizations, integrated video output and quad-pipeline 2D/3D acceleration. The board is designed for use in 0°C to +70°C operating environments. An onboard LM75 thermal sensor monitors local heat levels. For harsher environments special extended temperature testing is available. Pricing for the AtlasPMC/2 is \$2,500 in single unit quantities.

Curtiss-Wright Controls Embedded Computing, Leesburg, VA. (703) 779-7800. [www.cwcembedded.com].



Shelf Manager Module Improves Failover Handling

Because it was developed for the telecom market, it's not certain whether ATCA will gain any foothold in the military market. But the shelf management concept that's part of ATCA may have legs beyond strictly the ATCA space. Pigeon Point Systems offers its IPM Sentry Shelf Manager supporting the recent AdvancedTCA specification improvement that adds ShMC (Shelf Management Controller) cross-connects.

Adopted by PICMG in June, ShMC cross-connects dramatically improve redundancy by allowing the two shelf managers in an AdvancedTCA shelf to communicate with both of the Ethernet hub boards, rather than just one of them, as provided in the original AdvancedTCA architecture. Now, if a failure occurs in either an Ethernet hub board or in a shelf manager, a switchover of just the failed type of module is needed, which is much simpler and more reliable than coordinating a combined failover of both module types. The IPM Sentry Shelf Management Starter Kit

provides the hardware and software support for new shelf developers to build AdvancedTCA and CompactPCI shelves based on the IPM Sentry ShMM-500. The IPM Sentry ShMM-500 with ShMC cross-connect support is available now, with prices starting at \$350 each for 1,000 units.

Pigeon Point Systems, Scotts Valley, CA. (831) 438-1565. [www.pigeonpoint.com].



USB Module Delivers 12 A/D Simultaneous Input Channels

It took a while for USB to find its way into the embedded world, but now it's here. In the data acquisition realm it's become particularly useful. On the forefront of that trend, Data Translation announced the DT9836 Series of simultaneous analog input multifunction data acquisition modules for USB 2.0. The 12 separate 16-bit A/D channels on the DT9836 module guarantee less than 1 ns aperture uncertainty. All the analog and digital subsystem functions are sampled simultaneously to yield a data throughput of 225 kHz per channel.

Each analog input on the DT9836 has its own A/D converter to eliminate phase shift between channels, a common problem with a multiplexed architecture where all inputs share one A/D converter. All subsystems operate synchronously at 36 MHz, with 6 or 12 simultaneous, 16-bit analog inputs at 225 kHz per channel. Two 16-bit analog outputs are provided for waveform generation at 500 kHz per channel. And 16 digital input and 16 digital output lines enable external event synchronization. The DT9836 Series modules are available in two packaging configurations: a BNC connection box and an OEM embedded version with prices starting at \$1,295.

Data Translation, Marlboro, MA. (508) 481-3700. [www.datatranslation.com].



Software Tool Facilitates Complex HMI Designs

As cockpits, dashboards and control centers shift over to full graphic displays, Human-Machine Interface (HMI) design is getting a face lift all across the defense realm. Engenuity Technologies is releasing its next-generation VAPS software tool, VAPS XT, in response to emerging market requirements. The tool introduces cutting-edge concepts and capabilities for rapid design, testing and deployment of HMIs, such as avionics displays in airplanes.

VAPS XT interoperates with popular third-party solutions such as Telelogic DOORS and The Mathworks Simulink. VAPS XT integrates with nCOM, an innovative new toolkit that allows for easy connection with Engenuity's STAGE simulation products, thus providing HMI designers open access to a robust simulation system. Previously, developers required control over only a limited number of variables such as the color or line styles of displays. In contrast, VAPS XT features an unprecedented open and extensible architecture, giving users greater creative freedom and complete control over virtually every object parameter, allowing for limitless design possibilities.

The system provides the flexibility and control the company's HMI designers need when designing for complex requirements. Robust enough for demanding users, VAPS XT features fully integrated UML-based logic design using graphics-based state charts.

Engenuity Technologies, Montreal, Quebec, Canada. (514) 341-3874. [www.engenuitytech.com].



VME Plug-In Storage Module Does 320 Mbyte/s Transfers

Military applications such as high-speed data acquisition, high-definition imagery, telemetry recording and data mirroring are quite demanding when it comes to their rugged storage requirements. Beyond high density and ruggedness, they seek speedy data transfer rates. Satisfying such needs, Phoenix International Systems has introduced the first plug-in VME storage module with 320 Mbyte/s speed, its

Ultra320 SCSI VME Module. This new technology is available in a single-slot model (VL1-250-SC-DS-X) and a two-slot model (VL2-350-SC-DS-X), with capacity up to 600 Gbytes.

The new Ultra320 SCSI VME Module, which joins Phoenix International's extensive line of Rugged VME products, offers data transfer rates significantly higher than any other product on the market. The single-slot model can be configured with up to two each 73 Gbyte, 10K RPM hard disks; the two-slot model with up to two each 300 Gbytes, 10K RPM hard disks. Features include transparency to any operating system, an average Seek Read/Write of 4.1 to 4.5 ms at 10K, front panel and/or back plane SCSI connect, rugged steel construction with internal heat sink and 1,400,000 hour MTBF.

Phoenix International Systems, Orange, CA. (800) 203-4800. [www.phenxint.com].

PC/104-Plus Video Module Supports Many Display Types

Video displays are one of the important end-points that make up the U.S. Military's vision of a network-centric operation. After all, it's at the video display that the soldier, seaman or airman connects to that network. VersaLogic has announced the release of a new PC/104-Plus video module. The EPM-VID-3 offers high-performance add-on video output for embedded applications using the ATI Rage Mobility M1 graphics controller. It supports a wide range of display types, including desktop/CRT displays, LVDS flat panels and NTSC video monitors. It is suitable for use in security, defense, aerospace and other applications.



The EPM-VID-3 supports advanced embedded applications with resolutions up to 1600 x 1200 and 24-bit color.

Key features include 8 Mbytes of video RAM, up to three simultaneous display outputs and hardware-based MPEG-2 decoding. The module also boasts low power consumption, customizable video BIOS and

TV-out for NTSC-type monitors. TTL flat panel output is also available on custom versions of the product. The EPM-VID-3 is ideal for expansion of PC/104-Plus system, as a primary or secondary video device, or as temporary video output during system development and testing. The EPM-VID-3 is currently available from stock. Pricing is \$237 in OEM quantities.

VersaLogic, Eugene, OR. (541) 485-8575. [www.VersaLogic.com].



CompactPCI Board Boasts Onboard Cross-Bar Fabric

In today's high-performance military systems, speedy processing muscle alone isn't enough. A fast microprocessor is of limited use if there's no way to get data in and out of it fast enough to support such speeds. With that in mind, GE Fanuc Embedded Systems provides its CPC-7055 PowerPC-based CompactPCI single board computer. The bandwidth through the board's system controller is maximized by using 2 Mbytes of SRAM as a revolutionary "cross-bar fabric switch" allowing "any-to-any" connectivity of up to 100 Gbits/s of aggregate throughput, with non-blocking concurrent connections among all of the peripheral channels at full bus speeds.

The CPC-7055 utilizes the IBM 750GX PowerPC microprocessor offering processor speeds of 800 MHz or 1.0 GHz. Memory features of the CPC-7055 single board computer include up to 64 Mbytes of flash, up to 2 Gbytes of DDR 400 SODIMM memory with ECC support and an IDE interface for hard disk drive support allowing support of several types of data transfers. A CompactFlash socket is connected to the primary interface of the IDE controller. The board offers support for three 10 / 100 / 1000 Ethernet LANs and for the IEEE 1396.1 PCI common mezzanine card specification with two mezzanine card expansion sites. Pricing starts at \$3,119, and it is available immediately.

GE Fanuc Embedded Systems, Huntsville, AL. (800) 322-3616. [www.gefanuc.com].



PMC Board Supports the P4DP Variant of FPDP

The front panel data port (FPDP) interface is a popular data transfer solution for many military applications. But some applications need a bit more performance and can't support the complication of supporting FPDP cabling. Along those lines, Thales Computers unveiled its PMC-HTLK advanced high-speed serial data acquisition I/O mezzanine card.

Designed to meet the needs of the compact, real-time systems running on defense and aerospace applications, the PMC-HTLK offers high-speed data acquisition and point-to-point data transmission. PMC-HTLK is a 64-bit PCI mezzanine card (PMC) that is capable of moving high-speed data to and from PCI-accessible memory using a HotLink II transmitter channel, a HotLink II receiver channel or a 32-bit wide parallel data port P4DP. P4DP is a 32-bit rear-panel variant of the front panel data port (FPDP) that runs at a software-programmed clock rate of up to 40 MHz. PMC-HTLK supports three speeds—high speed (1 Gbaud) and low speed (350 Mbaud and 320 Mbaud)—and is available in commercial and rugged air-cooled and conduction-cooled versions. Pricing for the PMC-HTLK starts at \$2,690 subject to specifications.

Thales Computers, Raleigh, NC. (919) 231-8000. [www.thalescomputers.com].

Ethernet NIC Offers Low Cost 10 Gbit Solution

One aspect of Ethernet that military system designers love is its roadmap for even greater future bandwidth. Dynatem is now introducing "MAX Copper" (MaxCu), a single-port 10 Gbit Ethernet network interface card (NIC). The MAX Copper PCI NIC offers the highest throughput Ethernet performance in the world today. This product lets users employ low-cost CAT5e/CAT6 cabling for 10 Gbit Ethernet stacking and short-reach links (CAT5e and CAT6). Until now, only fiber-optic 10 Gbit Ethernet NIC solutions existed. Those short-reach fiber-optic NICs cost 30% more than our copper NIC and installed costs are dramatically reduced based on materials and installation time. MaxCu also consumes 50% less power than its fiber-optic relatives.



The MaxCu/10 Gbit Ethernet Server Adapter delivers industry-leading performance to bandwidth-intensive applications using a highly integrated PCI-X Intel 82597EX 133 MHz/64-bit 10 Gbit Ethernet controller coupled with a copper PHY from Vativ Technologies, the V10LAN transceiver/PHY. The MaxCu enables 10 Gbit Ethernet transmissions at distances up to 10 meters using standard CAT5e or CAT6 cabling and RJ-45 connectors. The Dynatem MaxCu/10 Gbit Ethernet Server Adapter provides standards-compliant Ethernet connectivity based on IEEE 802.3ae-compliant 10 Gbit Ethernet standard. Pricing for the MaxCu 10 Gbit Ethernet NIC ranges from \$2,499 to \$1,995.

Dynatem, Mission Viejo, CA. (949) 855-3235. [www.dynatem.com].



75W VME DC/DC Converter Features Low-Noise Specs

Low noise output and rugged design are top priorities in DC/DC converters in airborne, shipboard, ground mobile and C3I applications. Serving those needs, North Atlantic Industries (NAI) has announced the availability of a high power-density, single card slot, VME64 DC/DC converter. The 58KS1 provides up to 75 Watts of output power at full load over its operating temperature range of -40°C to +70°C, measured at the wedgelocks. It operates from a +5.0 VDC input and provides a +3.3 VDC output. The 58KS1 plugs into a standard VME64 backplane. The 58KS1 is designed and manufactured to NAVSO P3641 component derating guidelines and each unit receives ESS screening, including burn-in and temperature cycling. The unit is designed to meet the requirements of MIL-STD-461, when installed within the system.

Efficiency of the 58KS1 is 75% minimum. Noise and ripple is 33 mv p-p and output load transient recovery is 0.5 ms. The unit includes numerous fault protection features, including continuous short circuit protection—with automatic recovery—, output current limiting and output overvoltage protection. Voltage input and voltage output status signals and indicators are provided. Pricing for 100 pieces of the 58KS1 starts at \$1,754 each.

North Atlantic Industries, Bohemia, NY. (631) 567-1100. [www.naii.com].

PC/104-Plus Card Does 8-Channel JPEG 2000 Encoding

Remember when it took a whole rack of slot-cards to do motion video? Now military designers can do the same in a little PC/104-Plus card. Parvus announced availability of the CTR-1471 PC/104-Plus JPEG 2000 encoder card, a high-performance, eight-channel video compressor module supporting the enhanced features and quality provided by the JPEG2000-ISO/IEC15444-1 image compression standard. Designed to withstand extreme temperature operation (-40° to +85°C) and high mechanical stress, the CTR-1471 is an ideal solution for high-reliability and mobile video applications, including networked/wireless video and image distribution systems.

This board implements the computationally intensive operations of the JPEG 2000 image compression standard, as well as provides fully compliant code stream generation for most applications that support real-time video encoding. It contains a dedicated wavelet transform engine, three entropy codecs, an onboard memory system and embedded RISC processors to provide a complete JPEG 2000 compression/decompression solution. The board is able to process images at a rate of 40 Msamples/s in reversible mode, and at higher rates when used in irreversible mode. The CTR-1471 is now in stock and priced from \$765/each in quantities of 100+ units.

Parvus, Salt Lake City, UT. (801) 483-1533. [www.parvus.com].



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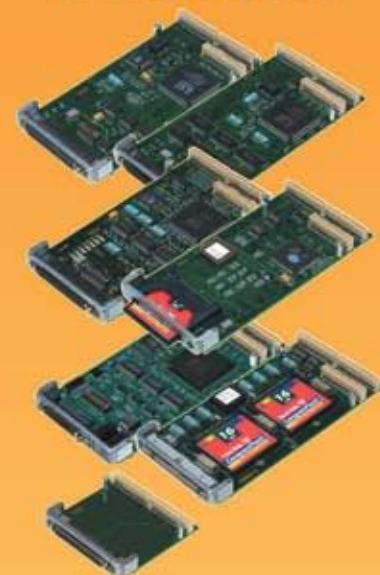
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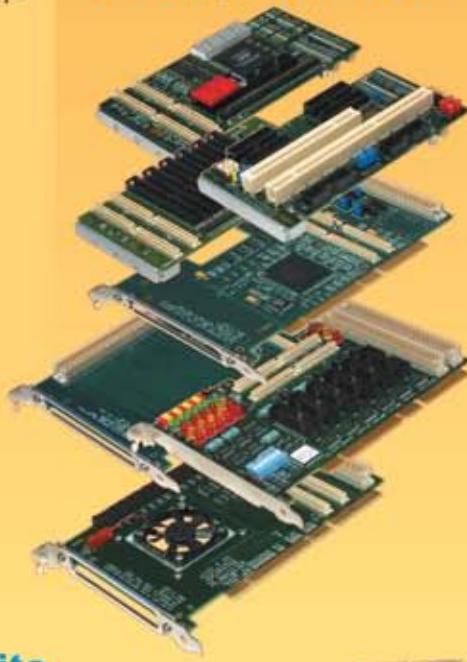
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COTS View

Drifts and Calibration: Fine Tuning Data Acq

Because no two military data acquisition subsystems are alike, it's important to choose a calibration strategy suited to the application.

Stephen Wenner, Senior Engineer

Myron A. Semack, Dir. of Software Engineering

RTD Embedded Technologies

Long gone are the days when data acquisition involved a person manually monitoring and writing down the status of some process to be analyzed later. Today, complex processes require data collection and data analysis to be done immediately and accurately. Whether the process is monitoring the position of ailerons, the pressure of a ground vehicle's oil fluid, or the temperature of the space shuttles' rockets, today's data acquisition boards are vital for collecting, digitizing and storing/transferring the right data at the right time.

Getting the right data requires an understanding of two types of errors that influence the overall conversion bit resolution of any data acquisition board: random and bias errors. For a deeper look into that area, see sidebar "For Effective Data Collection: Know Thy Error Types" on p.75 of this article. Random errors affect the precision of the data collected and can typically be reduced by acquiring a better data acquisition board and installing it in a properly shielded environment. Bias errors, however, affect the precision and are reduced through proper calibration of the board. Correcting those bias errors can be done through the two calibration techniques: manual and autocalibration. Manually calibrated analog I/O boards are widely used in the industry and in many situations offer rugged, reliable, consistent performance without software or hardware overhead. When manual calibration is not enough, two mainstream autocalibration methods exist: software calibration (SoftCal) and hardware calibration (HardCal). RTD Embedded Technologies has introduced a third method of auto-calibration, which is capable of both of these methods plus some additional features, in its SDM (Smart dataModules) product line: SmartCal (Smart Calibration).

SoftCal adds the ability to recalibrate without having to dismantle the data acquisition system, but at the cost of burden-

ing the CPU and some, if not all, of the surrounding computer buses. HardCal eliminates the SoftCal deficiencies by having the calibration execution resident on the data acquisition board. SmartCal advances HardCal by increasing the execution speed of the onboard calibration and any user-defined data processing programs through the use of a DSP. The increased execution speed compounded with operating system independent calibra-

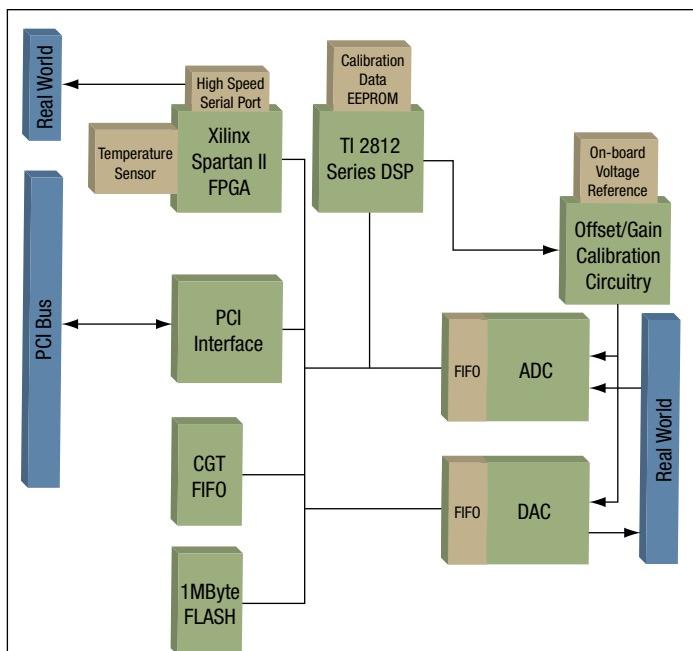


Figure 1

The SmartCal approach eliminates the drawbacks of SoftCal and HardCal by incorporating a DSP as the onboard processor for fast calibration of their A/D and D/A data paths, achieving calibration in under 300 ms. Since DSPs are optimized for mathematical computations, calibration can be performed much faster than with a microcontroller. And, since they are based on the HardCal principle, no user knowledge of DSPs is required—the process is transparent.



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tions expands the versatility and usability of the data acquisition board in a wider array of user applications.

Choice of Calibration Techniques

Both manual and auto-calibration follow the same general process: collect a large number of samples of a precisely known voltage, perform some filtering or averaging on the data, and determine if the measured voltage is the same as the actual voltage. If it is not acceptable, then adjustments need to be made to the circuitry and the process repeated. Though initial calibration of data acquisition boards occurs at the factory, regular adjustments may be required for continual precision and accuracy.

Manual Calibration

Less expensive, but highly effective, data acquisition boards require manual calibration of their mechanical potentiometers to adjust offset and gain errors. Manual calibration tends to be lengthy and requires external voltage references, but depending on the type of potentiometer used and the data collection environment, this type of calibration procedure will be suitable for many applications.

The manual calibration process involves powering up the data acquisition board for some period of warm-up time in a controlled thermal environment, connecting the analog inputs to a precision voltage source, reading the digitized voltage, and manually adjusting potentiometers until the converted voltage equals the precision source. These alignments require precision test equipment and step-by-step calibration procedures to ensure uniformity across the product line, being manufactured. This process needs to be repeated for the various gains and offsets. If a data acquisition board has analog output channels, then these too have to be calibrated using a similar method.

By setting each analog output to some value and measuring it with a precision voltmeter, the D/A (digital-to-analog converter) path offsets and gains can be adjusted until the output on the voltmeter matches the theoretical output of the converter. These resulting A/D and D/A calibrations may only be valid at the environmental temperature in which they were calibrated. Only if the characteristic thermal drift error of the board is less than the required resolution of the data being collected, can the manual calibration be relied on over other temperatures.

Users of manually calibrated data acquisition boards will sometimes profile the boards over the intended environmental



Figure 2

RTD's PC/104-Plus SDM7540 offers SmartCal features by utilizing the Texas Instruments TMS320F2812 DSP. There are sixteen single-ended analog inputs with a scan rate as high as 1.25 Msamples/s, 12-bit resolution, up to x64 gain and a FIFO. Complex scanning algorithms, including single conversion, multiple conversions, channel scanning, bursting and multi-bursting, allow the SDM7540 to collect comprehensive information not just pieces of data. This is accomplished through the use of a CGT (Channel/Gain Table) which stores channel, gain, polarity, range, single ended/differential, and skip bits for each data collection point taken.

temperature range it will be exposed to so that software corrections can be made for offset and gain drifts in post-data collection analysis. Auto-calibration is required when the user does not have physical access to the data acquisition board, when the user does not want to provide data correction software, or when the collected data is being processed in real time for immediate use and there is no time for corrective algorithms.

The SoftCal Approach

SoftCal data acquisition boards can be calibrated by executing a software routine within the host CPU. This is possible because the data acquisition board has onboard programmable digital-to-analog converters or digital potentiometers—instead of manual potentiometers—and onboard high-precision references. The data acquisition board is initiated by loading pre-defined factory hardware settings, which are typically stored onboard. The user has the ability through a host-side routine to recalibrate the board as necessary.

The process involves digitizing a number of samples of a high-precision voltage reference found on the data acquisition board, sending them to the CPU, calculating any deviations from the known value, and sending corrective data back to the data acquisition board so that digital potentiometers or D/A converters can be adjusted to correct for offset and/or gain errors. This process is repeated by the CPU

until the proper voltage reading is achieved. SoftCal data acquisition boards can be readily calibrated in the field with no external equipment required except the CPU.

One drawback to SoftCal is that a complex external routine must be integrated into the host-side application to perform the calibration when necessary. This may prevent the CPU from performing other tasks that are needed in the full-up system operation. CPU dedicated calibration time will be dependent on the data acquisition hardware, the calibration software routine and the CPU processing speed. The SoftCal software may also have compatibility issues with user-specific applications.

If a manufacturer's SoftCal data acquisition board is to be sold as a generic product to various users, it must support all possible operating systems—Linux, Windows, DOS and various RTOSes—compilers, for example Borland Turbo C++, Open-Watcom and others—and compiler versions. Binary modules are not a good solution because they are usually not portable across different compilers or between compiler versions. Though

language-neutral software frameworks such as COM or CORBA may be used to reduce many of these problems, these systems impose limitations of their own. The use of binary modules also can be a problem for customers using non-x86 CPUs. All of these drawbacks are solvable, but they require more effort by, and dependence on, the supplier of the SoftCal data acquisition board.

The HardCal Approach

HardCal data acquisition boards are SoftCal data acquisition boards with a processing unit residing on the data acquisition board. The calibration process is self-contained on the data acquisition board without the need of any special host-side software algorithm. The data acquisition boards can be recalibrated

For Effective Data Collection: Know Thy Error Types

In order for a user to ensure that the data collected for an application has the appropriate accuracy and precision, two types of errors that influence the overall conversion bit resolution of any data acquisition board must be understood. These are random errors and bias errors.

A random error is random noise that gets generated by each component on a board and by the actual design of the board itself. The magnitude of this error is dependent on the quality of the components chosen and the quality of the schematic design and PCB layout. Once the board is designed and manufactured, this error is fixed and can only be removed through data averaging. The resident A/D and D/A semiconductor chips set the best case conversion bit resolution for any data acquisition board. Manufacturers typically publish two numbers to describe this chip resolution: the marketing resolution and the theoretical resolution obtained under ideal conditions.

Depending on the quality of the part, and the environment it is operating in, the actual value will approach, but not achieve, the theoretical value at all input data frequencies. For example, one manufacturer's

8-bit converter may have a high noise floor at a particular input frequency that gives it an actual conversions capability of 7 bits. This is true whether you are talking about a 4, 12, 16, 24, or any other bit-level converter.

Bias errors are offsets caused by thermal drifts, temporal drifts and/or other sources. Typically these errors are calibrated out by the manufacturer before shipping to customers. As time progresses, and as the environmental temperature changes from where the board was calibrated, bias errors may become noticeable in sampled data. This drift can be minimized by using high-end components with high-stability coefficients over the expected environmental conditions that data is to be monitored.

If this is not possible then bias errors can be removed through recalibration, assuming this type of circuitry is available on the data acquisition board and it is user-accessible. If the bias error is due solely from thermal drift then the user also has the option of profiling the thermal drift of the board and using data analysis software to remove any errors. This method requires recording environmental temperature as well as the sampled data. This topic is covered under the Manual Calibration section.

How users choose to deal with random and

bias errors is dependent on their performance requirements and budget constraints, which may or may not be related. Performance is relative and dependent on the type of data the user is obtaining. If the data collection is for a short time period, the data acquisition board is in a stable environment and the resolution requirement is not high, then an inexpensive data acquisition board can be used to obtain reliable results. Using a more elaborate, expensive board would be overkill and could ultimately affect the board's Mean Time Before Failure (MTBF) or Mean Time Before Critical Failure (MTBCF) for the better or worse.

A more expensive board may indicate the use of more reliable components, but it could also mean more complex circuits, which can be possible points of failure. If the data collection is over a long period of time, at high speeds, in a wide, fast moving thermal environment, with each input channel having differing set-up parameters, then the data acquisition board may require high-end components and complex circuitry to meet these requirements. Sidebar Figure A summarizes the cost tradeoff for the type of data acquisition board used based on its susceptibility to thermal and temporal drifts.

If manual or auto-calibration is the desired means for minimizing bias errors so that the overall effective bit resolution of the data acquisition board can be realized, then very fine tuning components and circuits must be incorporated on the data acquisition board. By averaging sampled data, random noise can be eliminated revealing bias errors. These errors can then be reduced below the theoretical bit resolution of the converters.

Thermal Drift Error

Temporal Drift Error			Cost: Low → High
	High	Low	
High	<ul style="list-style-type: none"> • DAQ board in stable environment • Data taken over short period 	<ul style="list-style-type: none"> • DAQ board in environment where temperature varies over large range • Data taken over short period 	
Low	<ul style="list-style-type: none"> • DAQ board in stable environment • Data taken over long period 	<ul style="list-style-type: none"> • DAQ board in environment where temperature varies over large range • Data taken over long period 	

Figure A

Application requirements for data acquisition versus data acquisition offset errors, drift errors and cost.

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at will by the user or be set to recalibrate based on information received by a sensor such as a digital temperature sensor.

With HardCal, a one-line command on the host side can initiate a calibration of the data acquisition board by the onboard processor chip. Depending on the complexity of the data acquisition board, the SoftCal method can consist of hundreds or thousands of commands and may call several operating system-specific functions. The HardCal implementation is clearly easier to port across different platforms and requires less CPU overhead. HardCal offloads the difficult details of auto-calibration to the onboard processor, allowing software developers to focus on their applications. The user does not have to know anything about the data acquisition board's processor chip to perform this function.

In general, HardCal data acquisition boards have successfully used microcontrollers for the onboard processing chip. Unfortunately today's microcontrollers have limited processing speed and functionality and are not designed for math-intensive computations. This limits calibration speed and user application options.

"Smart" DSP-based Calibration

RTD has developed a product line known as SmartCal, which eliminates the drawbacks of SoftCal and HardCal by incorporating a Digital Signal Processor (DSP) as the onboard processor for fast calibration of their A/D and D/A data paths, achieving calibration in under 300 ms (Figure 1). Since DSPs are optimized for mathematical computations, calibration can be performed much faster than with a microcontroller. And, since they are based on the HardCal principle, no user knowledge of DSPs is required—the process is transparent.

The advantage of the SmartCal approach is that if needed, the user can unlock the full potential of the resident DSP by storing their own custom data processing application in the onboard flash. This feature means that the user now has the capability of higher-speed data processing and control compared to a microcontroller while reducing or eliminating CPU intervention.

The data acquisition board can be initiated to calibrate by having the host CPU board command the data acquisition board to calibrate itself by setting a register bit, by having the onboard data acquisition DSP autonomously initiate a calibration when it deems it necessary, or by having the data acquisition board send a Calibrate Interrupt to the host CPU board, which can then process the interrupt in an Interrupt Service Routine to determine when a calibration should start. An example of the second case would be the user storing a DSP program on the data acquisition board that sets upper and lower temperature limits for the onboard data acquisition temperature sensor, so that when the temperature goes out of bounds the data acquisition board will auto-calibrate.

SmartCal boards use DSPs over microcontrollers for good reason. The Harvard architecture of the DSP provides the multiple buses needed to simultaneously read an instruction, read a data value, process the instruction and write a data value. Because of their bus structure and internal multiply/accumulate

hardware, DSPs handle multiply/add cycles more efficiently than their microcontroller counterparts.

With multiple program/data buses and internal streamlining for mathematical operations, the data gets processed and moved around much faster than in a microcontroller. The Texas Instruments TMS320F2812 flash-based DSP has a 32 x 32-bit hardware MAC (Multiply/Accumulate) and 64-bit processing capabilities, making it extremely efficient in math-intensive applications.

Convergent Algorithm

Calibration by the DSP is performed by a sophisticated convergent algorithm that reads multiple onboard precision references and appropriately adjusts analog offsets to obtain accurate readings to within +/- ½ LSB. In order to avoid creating missing or duplicate digital codes, which can lead to non-linear resolution problems, the calibration is done in the analog signal path. Not doing this can cause a reduction in accuracy of your system above and beyond what a data acquisition board may specify. When calibration is finished, the DSP notifies the host by setting a status bit and/or generating an interrupt approximately 300 ms later. Since the DSP performs the calibration, it is operating-system-independent.

SmartCal boards are calibrated at the factory after a warm-up period, with the resulting set up values stored in an onboard EEPROM. As long as the board has not been recalibrated, these values will continue to be loaded as default values. Should the user decide to recalibrate, these new settings will be stored into a second location within the EEPROM. Restoration of the last known calibrated values occurs upon reboot. The user does have the ability to recall the initial factory defaults, if so desired.

Figure 2 shows an example of RTD's SmartCal boards, the PC/104-Plus SDM7540. This board offers SmartCal features by utilizing the Texas Instruments TMS320F2812 DSP. There are sixteen single-ended analog inputs with a scan rate as high as 1.25 Msamples/s, 12-bit resolution, up to x64 gain and a FIFO. Complex scanning algorithms, including single conversion, multiple conversions, channel scanning, bursting and multi-bursting, allow the SDM7540 to collect comprehensive information not just pieces of data. This is accomplished through the use of a CGT (Channel/Gain Table), which stores channel, gain, polarity, range, single ended/differential, and skip bits for each data collection point taken. There are two digital-to-analog outputs that can settle within 200 kHz. Each output has its own FIFO for data buffering, which can also be used as a signal generator without repetitive software overhead. During recalibration, the outputs are grounded so that the user does not have to disconnect analog outputs from servos, pumps or other devices. Once calibration is complete, the outputs are returned to a user-specified voltage. ■■

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COTS View

Extending the Life of Mission-Critical ICs

The small volumes on the military market are a mismatch to the high volumes and fast lifecycles that drive the semiconductor industry. Military system designers must look to specialist vendors and redesign options to keep pace.

Edwin Slipher, Chief Technologist
QP Semiconductor

Military-grade systems pose significant product lifecycle challenges. Military electronic components are simply not used in the volumes that commercial components are used. Personal computer and mobile phone manufacturers routinely deal with 10-million-plus product runs; but even high-volume military electronics, such as soldiers' personal radios, are sub-million quantities. Many programs have production runs in the tens to hundreds.

As long as military needs can piggyback on commercial production, parts are available. But commercial electronics products go through rapid product lifecycles. For instance, most computer products have six to nine month lifecycles and are essentially useless after three years. Short lifecycles in the commercial sector mean that certain ICs can be out of production—in other words, obsolete or EOL (end-of-life)—before the end of the military product lifecycle. Sourcing replacement ICs for these systems five, ten or twenty years down the road becomes a major challenge.

A requirement for a hand-held GPS or pocket calculator is an excellent example of an application where a commercial-grade product makes sense. Put bluntly, if the item fails, you buy a new one. There is no need for a repair depot, parts supplies and so forth. In comparison, an electronics system designed to be bolted into a combat platform, where field failure may cost lives, presents a different challenge. With the strict requirement of certain ICs that may now be obsolete, replacements simply can't be purchased commercially. The use of commercial ICs in such a product may be justified in some cases, but it presents significant cost burdens in ensuring long-term spare availability.

Fab Obsolescence

What is even worse than part obsolescence is fab obsolescence. Semiconductor companies have no manufacturing economic incentive to keep old fab lines operating. Costs are high and product demand is low. The fab machinery itself is out of production and becomes hard to repair. Nor can new fab lines run old processes. To do so, new masks are needed and a fab line

Options for Sourcing Obsolete/EOL ICs	
1. Find original parts.	Surprisingly, there are lots of old parts stored away in warehouses and supply depots. WWII-vintage new-in-box parts are still out there, as well as newer components.
2. Find original die.	Military contractors often buy bare die rather than packaged parts. When properly stored, bare die have a virtually infinite shelf life. Again, military specialty IC vendors can assist in both finding such die, and handling the packaging and test requirements.
3. Find other parts or die.	Parts made by second sources not originally qualified to supply parts for the particular product in question. However, in almost all cases, such parts will have to be formally qualified for the application, a potentially expensive task.
4. Re-engineer at some level.	Redesign in a way that eliminates the need for the unavailable part. This can occur in several ways: a. Design a replacement IC that can be manufactured in a current process. This is feasible with reasonable volume. The non-recurring engineering (NRE) cost has to be absorbed within the current year of production, in most cases, or funded separately by procuring activity. And naturally a re-qualification should be performed. Note also that multi-project (a.k.a. multi-die) wafers can make this cost-effective even at small volumes. b. Adapt a different component or process. c. Redesign the board to eliminate or replace the missing component. d. Redesign the system to replace everything.

Table 1

When supporting older designs, there are basically four strategies military OEMs can follow when faced with a need for obsolete parts. They are listed here, in order of preference.



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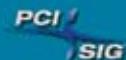
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that has been optimized for 300 mm wafers and a 130 nm process cannot manufacture the “huge” geometries of old processes measured in multiple microns.

In short, it's just not economical to keep exclusive military parts in long-term production. It's not easy to re-make them at a different fab either. Engineers who want to use commercially derived products in military systems should evaluate all of the issues and how they will play out during the total projected utilization life of the military product.

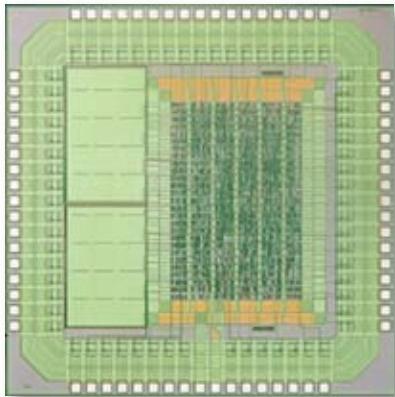


Figure 1

This QP Semiconductor part, QPALU, is an example of a redesigned ALU.

at the pros and cons of sourcing commercial parts. In a perfect world a simple solution would be to purchase and store enough inventory to meet the forecasted needs over the expected life of the product. This is hardly a practical solution given government procurement policies. Therefore, vendors must look elsewhere for alternative solutions.

This is where specialty IC manufacturers come into play. Military specialty IC companies meet stringent government quality manufacturing regulations and can advise and assist with issues of long-term storage of ICs, bare die or wafers. This sounds expensive, but it is highly cost-effective when compared to the costs of re-engineering components or systems years down the road. Table 1 explains the four strategies military OEMs can follow when faced with a need for obsolete parts.

Pros and Cons of Redesign

Component redesign is possible. Most ICs, however, have subtle process-dependant timing and parasitic characteristics that may not be documented. A redesigned part can be different in subtle ways. But if care is taken in the redesign, the differences can be eliminated or reduced to the point that the applications cannot detect them (Figure 1). Whether the design works in the system may be determined more by the system itself than by the initial specifications. Companies should select vendors who are willing to work through design issues to a satisfactory result.

The biggest advantage of a system redesign often lies in the ability to eliminate more than one hard-to-find component from a system (Figure 2). In some cases this can be invaluable.

Planning for IC Inventory

There are two sides to the problem. A military OEM who needs spares for an existing program is on the reactive side. And another military OEM who is planning a new program is on the proactive side. It's important to consider both sides and what the options are for each.

For new programs, vendors should look carefully



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However, the cost of formal re-qualification is significant in both time and dollars, with no absolute guarantee of success.

In most cases, planners should allow time and budget for re-qualification. The type, level and cost of a re-qual will vary with each application, but unless a vendor is fortunate enough to find military parts from the original approved vendor, and with a traceable history, some level of re-qual will be required.

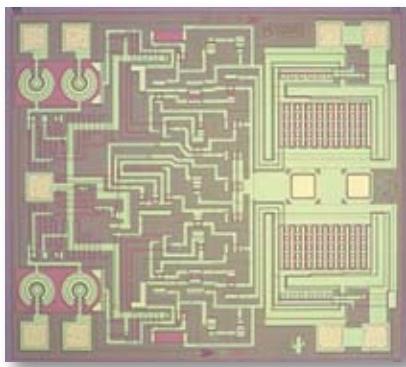


Figure 2

This QP Semiconductor part, the QP163x, is a redesign from a multi-die wafer: one device integrated from four.

fab shutdowns and other factors mean there may not be an opportunity for a final buy. For example, this April and again in August, National Semiconductor made five part numbers "no longer available" without offering lifetime buys (DS1691AJ, CLC402 MD8, CLC402 MDS, CLC420 MDC and CLC426 MDC).

Planners should consider working with a specialty military vendor to acquire sufficient stock before it is too late. By stocking up on mil-qual die as well as packaged parts, these specialty vendors can adapt to meet your needs. What should you look for in such a specialty vendor? First and foremost, experience. Vendors who have been in this business for years know the process better than recent entrants. Second is military qualification in IC fabrication, packaging and test. Lastly, experience in the proper storage of wafers and bare die. They last virtually forever if properly stored, but can be rendered useless by improper storage.

In short, the best strategy is to plan ahead. Regardless of component sourcing philosophy, ICs don't stay in production forever. Semiconductor manufacturers are often unaware that parts are being used in military applications and therefore have no incentive to announce a pending EOL other than to their primary market base. You need to plan for this eventuality. And you want a partner who has experience in multiple solutions so you can choose the best for your design requirements. ■■

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Vendor Selection

Specialized military-qualified vendors have entered the market to assist companies in finding and packaging die for these applications. Semiconductor companies usually offer lifetime buy opportunities for most products, but such an opportunity is neither guaranteed nor legally required. Variations in yield,

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Coming Next Month

We have to move fast here at *COTS Journal* to keep you briefed on the exciting key technology trends critical to military system designers like you. It's a labor of love for us, but we often reach December with a level of shock at how fast the year has sped by. This year is no different. Where has the time gone? Here's what's on deck for our December issue:

- **VME Single Board Computers.** As VME approaches its 25th birthday (next year), it's keeping ahead of the performance curve by riding the wave of the various switched fabrics. As these get rolled into VSO specs such as VITA 41, VITA 42, VITA 46 and others, efforts remain to keep VME as compatible as possible with previous generation boards, backplanes and boxes. This feature section explores the details behind those trends and updates readers on the technology trends shaping VME SBCs.
- **Serial Switched Fabrics.** Switched serial fabric technologies—PCI Express, InfiniBand, Serial RapidIO and others—continue to vie for position as the favorite for high-end military embedded computing applications. This section explores how system designers can benefit from the marriage of switched fabrics with embedded computing form-factors like VXS, MicroTCA and AMC.
- **Designing for EMI/RFI.** With the era of GHz interconnect and processors speeds squarely upon us, the task of managing electromagnetic interference (EMI) and radio frequency interference (RFI) has become more of a challenge. Articles in this section focus on reducing and eliminating EMI/RFI effects in enclosure and embedded computer designs.
- **PC/104 in the Military.** With its blend of compact size and inherent ruggedness, PC/104 continues to gain fans in the military realm. This Tech Focus section updates readers on PC/104 SBC boards and provides a product album of representative PC/104 SBC products. A special expanded product directory of PC/104 boards will be provided on our Web site.

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Editorial

Jeff Child, Editor-in-Chief



The UAV Gold Rush

Voicing his plans to crackdown on out-of-control costs, Air Force Chief of Staff Michael Moseley was quoted last month in CongressDaily, tossing around some clever “gold” metaphors. “I don’t believe Congress will be sending unsolicited pots of gold to the Department of Defense,” Moseley said. While not discussing specific programs, Moseley remarked that the service has little tolerance for systems that do not meet cost and schedule goals, and acknowledged that some pricey programs may face his own budgetary ax. There’s no question that the Air Force is developing some of the military’s most expensive programs, including the F/A-22 Raptor and the Joint Strike Fighter. Meanwhile its aircraft inventory is over two decades old, driving the need to buy new refueling tankers, cargo aircraft and fighter jets. But in the increasingly constrained budget environment, it just won’t be practical to replace aircraft one for one.

Moseley also expressed that he wants to buy more unmanned aerial vehicles (UAVs). The U.S. Air Force plans to expand the number of Predator UAV squadrons from 3 to 15. The Global Hawk unmanned aircraft is “worth its weight in gold,” Moseley said. UAVs have certainly proven themselves a good investment so far. Consider that UAVs comprise only around 11 percent of the total DoD annual budget, even though they make up an impressive 81 percent of all the U.S. Military’s aviation hours flown per year. Air vehicles without humans aboard, UAVs are a success story across all branches of the U.S. Military, and all are ramping up their numbers. The Army alone had seven UAVs in 2002, but grew that number to 333 this year, and have 437 planned for 2006 with the trend continuing upward.

Meanwhile, overall interest in UAVs is skyrocketing. According to market research firm Forecast International, the worldwide market for UAV Reconnaissance Systems—including air vehicles, ground control equipment and payloads—is expected to be worth \$13.6 billion through 2014. Of that total, the United States is by far the largest single market. American firms have a value share of more than 50 percent of this market and could gain control of a further 5 to 10 percent over the next decade. More than 9,000 UAVs are expected to be purchased over the next 10 years by countries in every region of the world. That number, says the market report, doesn’t include funding for RDT&E and operations and maintenance in its analysis, but as procurement increases, money spent in these areas is also likely to increase.

The growing UAV demand is great news for vendors of embedded modular computers. That’s because computing and

communications technologies—particular those that ride the wave of commercial technology developments—are the two key enablers of UAVs.

The two basic approaches to implementing unmanned flight, autonomy and pilot-in-the-loop, rely predominantly on microprocessor and communication (data link) technology, respectively. And while both those strategies are used to differing levels in all of today’s fielded UAVs, it is these two technologies that compensate for the absence of an onboard pilot and thus enable unmanned flight. Advances in both depend on commercial markets, the PC industry for microprocessors and memory—just as embedded computers such as VME and CompactPCI do—and the wireless communication industry for data protection and compression.

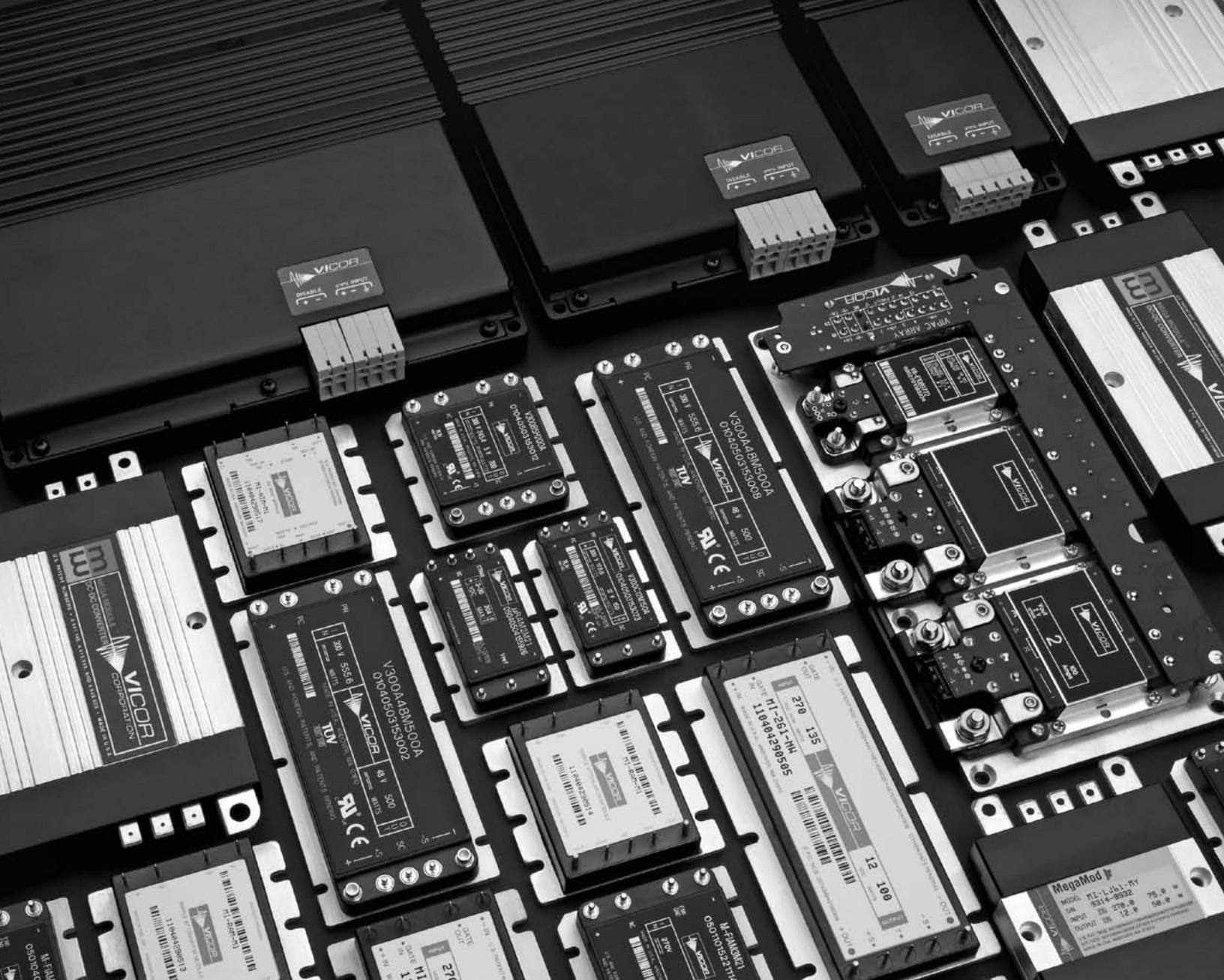
Despite its lucrative market opportunities and the attractive capabilities UAVs offer, the UAV Gold Rush is not without its downside. The fast moving pace of development seems to be moving ahead without taking into account the limited interoperability between different UAVs (and between UAVs and manned systems) and with the wider user community. The DoD is starting to acknowledge those downsides in their roadmap plans. The Secretary of Defense’s UAS Planning Task Force cites in its Unmanned Aircraft Systems Roadmap how many UAVs have been developed with limited attention to Joint interoperability requirements. As they become the predominant collection systems across virtually every echelon of command, it’s vital to coordinate, share and integrate them into the larger warfighting community.

The UAS Roadmap report also explains that as UAVs continue to improve their range and communications capability, there’s no need for them to serve a single user or even a single Service Branch. Although UAVs have proven themselves of tremendous value in current combat operations, there are many deficiencies in several areas including lack of standard communications frequencies and waveforms, lack of standardized sensor products, lack of standardized meta-data for both sensors and platform information, and lack of a common tasking system that crosses the traditional command boundaries.

To me, that all points to more opportunities for standards-based UAV computing platforms that can be leveraged across different UAV families and UAV mission payloads. Without such standards-centric thinking, UAVs are likely to face the same problem that occurred in the military radio area—where a mass of incompatible devices led to an inefficient mess. If UAV development continues on a fragmented course, well...it wouldn’t be the first Gold Rush in history to get out of control and go awry. ■



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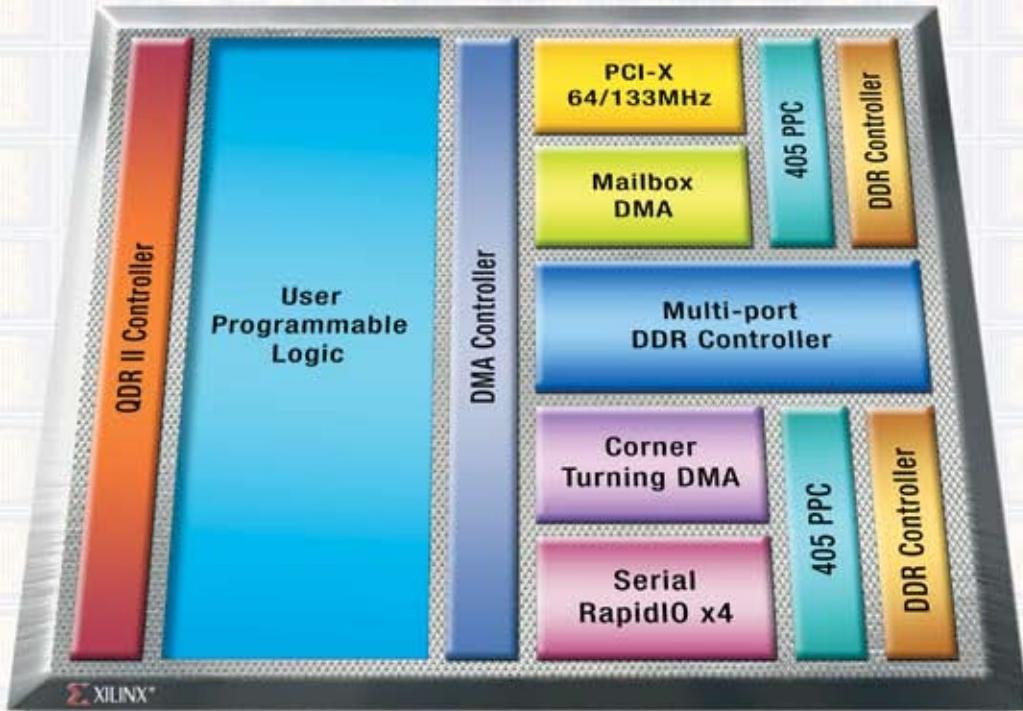
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